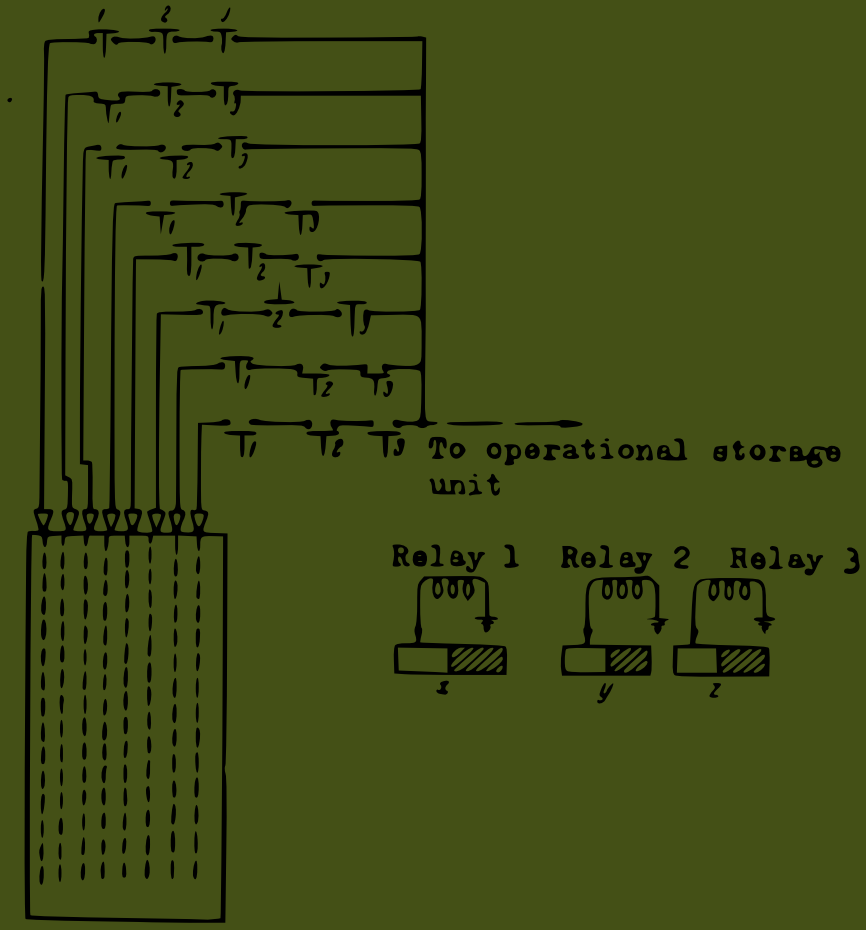
S.A. Lebedev

COMPUTER ENGINEERING



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EDITORIAL NOTE

This publication is concerned with a series of questions in computer engineering: the power supply system of the high-speed electronic computer of the Academy of Sciences of the U.S.S.R.; new elements and units for computers; a method of control of the arithmetic unit; a method of selecting the required word from the dictionary in machine translation; and present-day computer terminology.

The publication was drawn up by specialists in the design and working of electronic computers.

Besides papers from the Institute of Precision Mechanics and Computer Engineering, this publication contains articles by authors from other organizations concerned with computer engineering.

O. K. SHCHERBAKOV

THE POWER SUPPLY SYSTEM OF THE HIGH-SPEED ELECTRONIC COMPUTER (BESM) OF THE ACADEMY OF SCIENCES OF THE U.S.S.R.

Questions of the reliability of working of high-speed electronic computers have recently become of increasing significance. The reliability of working of a machine depends to a considerable extent on the operation of the power supply installations.

During the period of operation of BESM (1952 to 1955), observations were made of the operation of the separate installations of the supply system and also of the system as a whole. Besides these observations, a series of experiments was carried out which made it possible to record the characteristics of the system and to establish certain peculiarities in its operation. Methods of supply which facilitated the detection of incipient faults in the elements of the machine were also investigated. This made it possible to propose ways of simplifying the existing supply system, and also to make recommendations which may be useful in the design of supply systems of other machines and installations similar to BESM.

All the installations in the power supply system of the machine fall into one of two groups: heater supply to the valves, and d.c. power supplies.

Fig. 1 is a block diagram of the heater power supply for the valves of the machine. The system consists of a three-phase 220 V supply, a regulated oil-filled auto-transformer (ATMK 100/0.5), a ferro-resonant voltage stabilizer, step-down transformers, and a d.c. motor-generator with an output of ±6.3 V.

A second group of installations provides d.c. power supplies for the machine at all required ratings, and includes d.c. motor generators, rectifiers, storage batteries, a rack for the control of generator voltages and racks of electronic stabilizers.

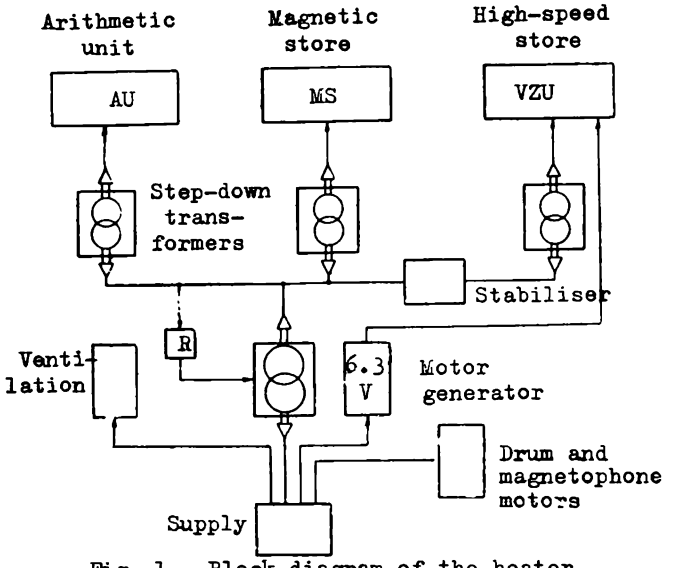

Fig. 1. Block diagram of the heater supply.

The power requirements of individual racks and of the whole machine are shown in Table 1.

In general, the following types of valve are used: the 6F8 double triode, the 6AC7 pentode with a short characteristic, the 6AG7 amplifier pentode, and the 6L6 beam tetrode. These are all normal receiving-valve types which are widely used in radio circuits.

In designing the power supply system, particular attention was devoted to securing maximum reliability in its working. Faults which may appear with variations of the heater voltage in operation are as follows.

With variation of the value of the heater voltage the emissivity of the cathode changes; therefore the anode currents change. With prolonged operation of the valves the cathode emission deteriorates. The anode current decreases with time to such an extent that the valve no longer satisfies its specification, and the correct working of the machine is interfered with. From this point of view the valve may be characterized by the emission characteristic $I_a = \Psi(V_f)$, and the observation of the

TABLE 1

Power requirements in kW

Voltage ratings (V)	AU	MS	VZU	Whole machine
Central d.c. supply				
+300	3.0	1.0	0.5	4.5
+200	3.6	1.4	1.0	6.0
+100	2.0	0.1	0.4	2.5
+110	-	-	-	0.7
+100	2.0	0.5	1.0	3.5
+400	0.08	0.04	0.08	0.2
Special d.c. supply				
+400	-	-	1.0	1.0
+40	-	-	0.07	0.07
+20	-	-	0.08	0.08
-300	-	-	0.5	0.5
-1300	-	-	0.5	0.5
-1700	-	-	0.5	0.5
Total d.c. power	10.68	3.04	5.58	20.0
Heater supply				
200	17.0	5.0	3.0	25.0
+6.3	-	-	7.0	7.0
Ventilation	-	-	-	23.0
Total power requirement	27.68	8.04	15.58	75.0

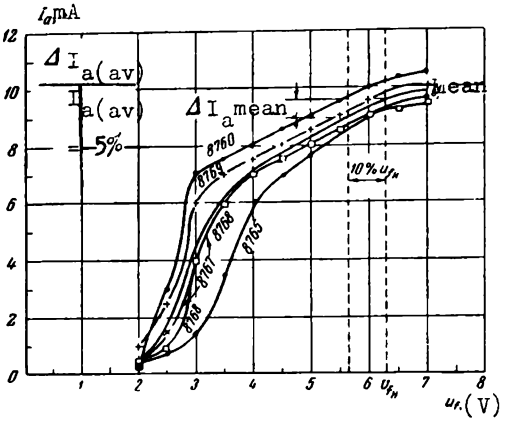

Fig. 2. Characteristics of 6AC7 valve (0 hours).

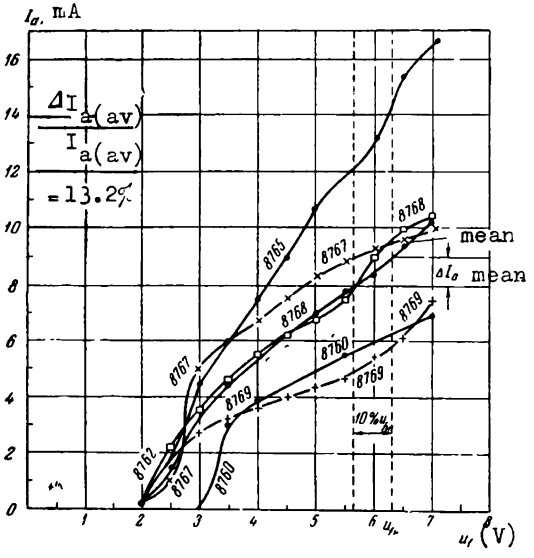

Fig. 3. Characteristics of 6AC7 (6500 hours).

change of this characteristic in the course of a long period of operation is of great interest (Ref. 1).

To this end we took the emission characteristics of the basic types of valve used in the machine immediately after switching on and also after 6500 hours of operation.

The anode currents of a number of 6AC7 valves were plotted against heater voltage initially and after 6500 hours of operation. The curves obtained are shown in Figs. 2 and 3 respectively. Similar curves for 6F8 valves are shown in Figs. 4 and 5. It is seen that

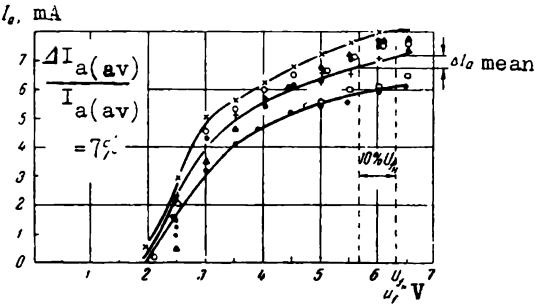

Fig. 4. Characteristics of 6F8 showing spread and average values (0 hours).

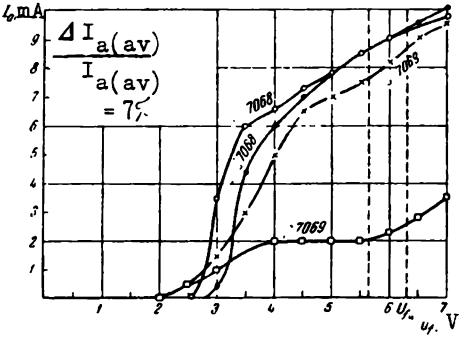

Fig. 5. Characteristics of 6F8 (6500 hours).

reduction of the heater voltage by a certain amount gives a different reduction of the anode current, initially and after a long period of operation. With length of life the anode current becomes more sensitive to cathode underheating. Thus when the heater voltage of the 6AC7 is reduced by 10%, in new valves the anode current drops on the average by 5%, but in valves which have run for 6500 hours it drops by 13.2%. For the 6F8 the corresponding figures are 7% and 13.5%. The results for individual 6AC7 valves are given in Table 2. These percentage decreases in anode current become still more severe with further operation of the valves, since the steeper part of the characteristic moves progressively to the right and approaches the rated heater voltage of the valves.

TABLE 2

$\Delta I_a/I_a$

Valve No.	0 hours	6500 hours
8760	4.9%	11.4%
8765	7.6	17.0
8767	4.9	6.3
8768	4.9	17.7
8769	4.9	16.7
8762	-	13.2
Average	5.0	13.2

We have also carried out a test of the stability of operation of the standard elements of the machine in relation to change of heater voltage (Ref. 2). A block diagram of the test circuit is shown in Fig. 6. The circuit simulates the actual operating conditions of the elements in the machine.

The test circuit consists of a small loop and a larger loop. The small loop, which is in circuit when the switch (PT2) is in position 1, contains pulse elements: the pulse shaper (F), the transfer circuit (Ts), and the gate (V). The large loop, with the switch in position 2, contains, besides pulse elements, the potential inverters (Ia) and (Ib), the flip-flop (T), the cathode followers (Ka), (Kb), and the diode follower (D).

Testing of the elements was carried out by means of the large loop and also the small loop, with PT2 in the appropriate position.

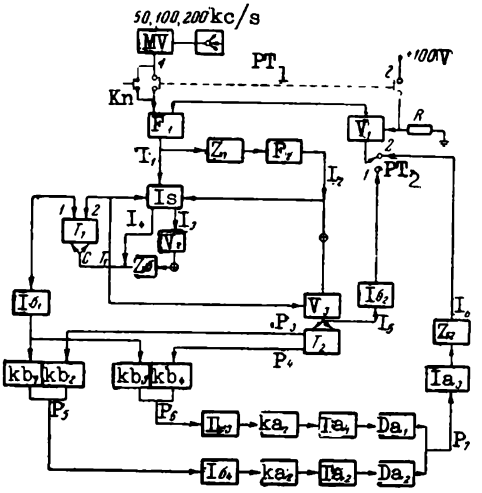

Fig. 6. Block diagram of test circuit. A = attenuator.

The principle of operation of the system is as follows: with the switch PT2 in position 1, pulses with a frequency of 50 to 100 or 200 kc/s are fed by the multivibrator (MV) to the pulse shaper F1 and thus to the assemblies Ts and Z1, from which, with a delay of 2.5 μsec, they enter the second input of Ts.

The pulse I4 from the output of Ts triggers the flip-flop T1 into position 0. The signal from one side of T1 is supplied to the third input of the assembly Ts and also to V3; the signal from the other side of the flip-flop is supplied to the input of assembly Ibl.

The pulse I3, entering the input of T1 from assembly Ts with a delay of 0.6 μsec, triggers the flip-flop into position 1, and the potential across V3 opens it to a signal supplied from F2. The signal from V3 enters the pulse shaper F1 by way of Ib2 and V1, and so the system repeats its cycle of operation so long as PT2 is in position 1.

To work the large loop, PT2 is changed to position 2.

As we have shown, potentials are applied from the output of T1 to Ib1 and V3. The pulse obtained at the output of V3 triggers the flip-flop T2. Signals from T2 and from the inverter Ib1 enter the cathode follower assemblies Kb, which are connected by a coincidence circuit. From the outputs of Kb, signals enter assemblies Ib, Ka, Ia, and D, are then added and enter the delay unit Z2 through Ia3, whence the signal, delayed by 2.5 μsec, enters the pulse shaper F1 through the gate V1.

Tests with change of heater voltage were made separately for each standard element being tested. Tests were made on ten units of each type. The limits of change of heater voltage were determined either by cessation of working of the whole system or by deviation of amplitude of the output pulse by 32% or of the output potential by $\pm$ 7%. (These limit figures are taken from the tolerances of signal amplitude accepted for BESM).

Examples of the relations obtained during tests on elements Z and F are shown in Figs. 7 and 8. Each of these graphs can be divided along the heater voltage axis into two regions: the region of stable working (1,2) and the region of instability or failure to operate (3).

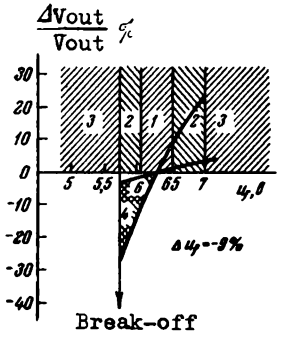

Fig. 7.

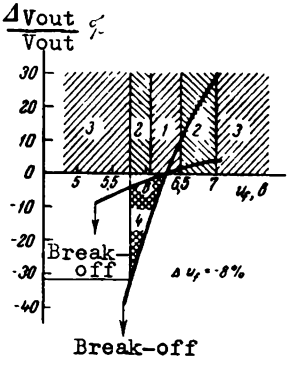

Fig. 8.

The region of instability corresponds to heater voltages in the case of which normal working of the separate elements is disturbed. The region of stable operation

can be divided into two parts: the first (1) corresponds to the region of changes of heater voltage which are admissible in routine operation of the machine; and the second (2) is used for preventive testing. If region (1) is made relatively wide, then the more often should preventive testing of the apparatus be carried out; but less stringent demands are made on the stability of the power supplies. Region (4) is bounded by the limit characteristics of the elements being tested. The characteristics of all remaining elements lie within this region.

In this way the required stability of the heater voltage supply for standard elements was established within the limits of 3 to 4%. Reduction of heater voltage by 7 to 12% was accepted for preventive testing.

At present, preventive testing of the machine by special programmes with reduction of the heater voltage is the main test of the reliability of operation of BESM. A 10% reduction of heater voltage is used.

With increase of heater voltage the amplitude of spurious signals increases considerably; therefore, this test is resorted to only in order to detect elements which are transmitting spurious signals. For this test the heater voltage is increased by 7 to 12%.

For stabilizing the heater supplies of cathode-ray tubes, ferro-resonant stabilizers are used. The total instability of this system does not exceed ±1%, which is perfectly admissible for the heater supply of tubes. For the heater supply of the valves in the high-speed storage system VZU, a d.c. motor-generator is used. The use of direct current for the heater supply of the valves of this rack is indicated because direct current does not set up alternating magnetic fields, and so permits less elaborate screening of the tubes. When using alternating current for the heater supply of the valves, we observed an abrupt deterioration in the working of the unit because of displacement of the beam in the oscilloscope. This occurred despite the fact that mutual compensation of the magnetic fields set up by the heater current, which spread out over the chassis and panels of the rack, had been provided for.

However, with recent improvements in the installation system of the rack and of the screening of the tubes, it will be possible to supply the valve heaters with alternating current.

With abrupt switching on or off of the heater voltage, the reliability of operation of the machine decreases. It is necessary that the rated thermal conditions in individual valves and in the racks of the apparatus shall be attained gradually, and a smooth rise and fall of the heater voltage must be provided. This restricts the value of the initial current, and at the same time provides the possibility of decreasing the heater voltage during preventive testing of the machine. Since the operational reliability of the machine decreases with frequent and sudden switching off of the heater voltage, the installations for the heater supply of valves must be reliable, and capable of giving an uninterrupted supply throughout prolonged periods of operation - say, several weeks.

The machine is operated from a 220 V 50 c/s three-phase supply. Naturally, the parameters of the mains supply can have a considerable influence on the stability of the machine. Observations of the mains supply have shown that the voltage is constantly changing. Thus, in the course of 24 hours we recorded rises of up to 10 or 15%, and drops of as much as 25 or 30% below the nominal value.

It became clear that a unit had to be installed between the mains supply and the machine, to maintain the heater voltage within the specified limits. To this end we installed an oil-filled auto-transformer ATMK-100/0.5. With a rated voltage of 220 V on the primary, the minimum secondary voltage is about 22 V. With 33:1 step-down heater transformers, the heater voltage is 0.67 V. Switching on the machine with a voltage of this value is perfectly safe. The heater voltage is then increased smoothly to the rated voltage of 6.3 V in the course of 15 to 25 minutes, and is maintained at this value with an accuracy of 3 to 4% by an electronic regulator (R in Fig. 1).

To test the effect of a momentary lowering of the mains voltage on the stability of the machine, tests were carried out by means of artificial transients in the mains supply while the machine was working on a programme. In the course of these tests we did not observe any dislocation in the operation of the machine, even when the mains voltage was reduced during one second to 150 to 170 V.

Analysis of the a.c. supply installations of the machine has permitted us to draw the following main conclusions:

a) Transients in the supply which may arise when

extraneous loads are switched on do not cause dislocations of the operation of the machine.

b) Deviation of heater voltage for standard elements of the machine of not more than ±3 or 4% is admissible. Stability of this order is provided by an auto-transformer with an electronic regulator.

c) Deviation of the heater voltage of cathode ray tubes of not more than ±1% is admissible. This can be achieved by the use of ferro-resonant stabilizers placed after the auto-transformer.

d) For preventive testing of the machine, a change of heater voltage of ±10 to 15% from the rated value is recommended.

The second group of power supply installations provides the operating conditions of the electronic automation elements. All elements of the machine fall into one of two classes: pulsed or non-pulsed. The pulsed elements are radio-engineering systems of the pulse amplifier type; the non-pulsed elements are radio-engineering systems of the d.c. amplifier type. Demands on the elements of the machine are heavier than those occurring in radio installations. Considerable length of life is required of them, with reliable operation throughout; and, also, there is a wide range of input pulse amplitudes, and considerable output powers may be required.

Demands on power supplies are also heavier than in the case of radio installations. The reliability of the machine, determined by the stable working of the elements, depends on the characteristics of the supply sources and installations. The principal features of the d.c. supplies are considered below.

The voltage ratings shown in Table 3 are those necessary for the power supply of the machine.

The basic voltages are used for the supply of standard elements. The voltage of ±110 V serves for the supply of the automation and protection circuits, and the special voltage ratings serve for testing the efficiency of elements of the machine. Supply voltages of high stability are essential for the cathode ray tube storage installation VZU. Their stability is ±0.1%. This order of stability is essential, since precise deflection of c.r.t. beams is of great importance for the correct

TABLE 3

Basic supplies (V)			Special ratings (V)
From central power supply	High stability supply	From dividers of individual racks	
+300	+ 400 - 300	+ 110	- 96
+ 200	-1300	+ 2	- 98
± 110	-1700	- 14	- 380
+ 100	+ 40	- 50	- 420
- 100	+ 20	- 58	
- 400			

working of the high-speed store. It is essential that, whatever the read-out repetition frequency of any one point, and whatever the instability of the mains supply, the beam should, for one and the same address code, fall strictly on one and the same spot on the tube screen (Ref. 3). Taking the diameter of the beam to be d = 0.7 mm, we can allow a shift of the centre of the spot of 0.07 mm in repeated deflections, giving an overlap of the areas of the spots of 88%. The maximum possible displacement of the spot (0.1 mm) corresponds to an alteration of voltage between the deflector plates of 0.28 V (with a deflection sensitivity of 0.35 mm per V).

The maximum alteration of position of the spot produced by a change of 1% in the supply voltage is as follows:

$$-300\ \text{V} \qquad \Delta_1 = 0.055\ \text{mm}$$

$$+400\ \text{V} \qquad \Delta_2 = 0.065\ \text{mm}$$

These values were obtained experimentally with the aid of a special compensation system. The maximum change of position of the spot with a change of 1% in the voltages supplying the deflection system is:

$$\Delta_{\text{defl}} = \Delta_1 + \Delta_2 = 0.055 + 0.065 = 0.12\ \text{mm}.$$

The required stability of the voltages supplying the deflection system is:

$$\Delta_{\text{defl}} = \Delta_{\text{total}} - \Delta_{\text{accel}},$$

where Δ_{total} is the admissible displacement of the spot, which, as we have shown above, is 0.07 mm. Δ_{accel} is the shift of the spot caused by instability of the accelerating voltages supplying the tubes. The shift is proportional to the variation of the voltages, and will be greatest at an extreme point on the signal plate (60 mm from the centre).

With an instability of the accelerating voltages of 0.1%, $\Delta_{accel} = 0.1 \times 10^{-2} \times 60 = 0.06$ mm. Hence the admissible displacement of the spot on the optimal plate, depending on the instability of the supply voltages of the deflecting system, is

$$\Delta_{defl} = \Delta_{total} - \Delta_{accel} = 0.07 - 0.06 = 0.01 \text{ mm},$$

which corresponds to an instability of the voltages supplying the deflecting system of ±0.1% (Ref. 4).

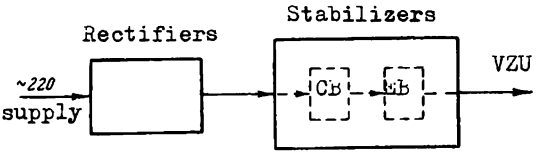

Fig. 9. Block diagram of stabilized power supply sources. CB - control block; EB - executive block.

Stability of these voltages is secured by the use of electronic stabilizers, which are set up according to a modular system, with maximum use of individual elements.

Fig. 9 is the block diagram of the stabilizers. The installation consists of a rack of rectifiers and a rack of stabilizers, in which, as a rule, the control and executive systems are set up as individual blocks. Selenium rectifiers are largely used in the rectifier rack. Individual rectifier installations are assembled on pull-out chassis, which allows rapid replacement and repair. The series stabilizer valves are of the type 6N5S, with up to 16 valves in parallel to provide a current of 4 A. The stabilized power supply sources are assembled in racks.

In order to discover what instability of the supply voltages is admissible, an investigation was carried out on the stability of working of individual standard elements of the machine.

TABLE 4

Standard element	Limits of stability of operation (%)	Voltage (V)			
Flip-flop T	±5	+200	-100	-58	+100
Pulse shaper F	±8	+100	+200	-50	+2
Gate V	±5	+200	+100	-100	
Inverter Ia	±3	+110	-400	-100	
Inverter Ib	±5	+110	-400	-100	
Amplifier with delay	±9	+200	-15		
Cathode follower K	±10	+300	+200		
Transfer circuit Ts	±14	+200	+100	-100	

Experiments with the alteration of supply voltages were carried out separately for each standard block tested and for all assemblies. In testing blocks of any one type, the operating regime of the remaining standard elements was left unchanged. Pulse amplitude matching between elements was brought about in accordance with the requirements of normal working of the machine. The block diagram of the test circuit is shown in Fig. 6.

The tests made it possible to draw up graphs similar to those shown in Figs. 7 and 8, which have already been discussed. Data on the limits of stability of individual elements are shown in Table 4.

Besides this, the operation of the machine was tested by a set programme, with lowering and raising of individual d.c. voltages. Data are shown in Table 5. It follows from Tables 4 and 5 that for reliable operation of the machine a stability of the supply voltages of not less than ±2% is necessary over prolonged periods (Ref. 1). Subsequent observations in the course of a two-year operation of the machine confirmed these conclusions.

To obtain voltages of this stability, a central d.c.

TABLE 5

Voltage ratings (V)	Limits of deviation		Frequency kc/s	Result to programme
	V	%		
-100 +100	-98 +102	-2 +2	400	Proceeds
-100 +100	-96 +102	-4 +2	400	Proceeds
-100 +100	-96 +104	-4 +4	400	Proceeds
-100 +100	-95 +104	-5 +4	400	Proceeds
-100 +100	-95 +98	-5 -2	400	Proceeds
-100 +100	-95 +105	-5 -5	400	Stops
-100 +100	-105 +105	+5 +5	400	Stops
-100 +100 +200	-103 +103 +205	+3 +3 +2.5	400	Proceeds
-100 +100 +200	-103 +103 +210	+3 +3 +5	400	Proceeds
-100 +100 +200	-103 +103 +190	+3 +3 -5	400	Stops
-100 +100 +200	-104 +104 +195	+4 +4 -2.5	400	Stops
-100 +100 +200	-95 +104 +205	-5 +4 +2.5	400	Proceeds with dislocations
-100 +100 +200	-98 +102 +205	-2 +2 +2.5	400	Proceeds stably

power supply has been created for the machine. The central power supply consists of five d.c. generators with electronic regulators, and a bank of trickle-charged storage batteries. The electronic regulators are assembled in one rack. The block diagram of the central power supply is shown in Fig. 10.

It was at first supposed that abrupt switching of the d.c. voltages would reduce the life of the valves, and thus the reliability of the machine. However, operation of BESM has shown that, with correct adjustment of operating conditions, and with preventive checks of the units, switching the d.c. voltages on or off does not affect reliability.

On the other hand, failure of one of the voltages (excluding the high-voltage supplies for the tubes, which are switched on separately) often leads to a group of elements getting out of order, and is therefore

inadmissible. To preclude this, a minimum cut-out, which disconnects all the d.c. voltages if one of them fails, and a special safety device which prevents switching on of d.c. voltages before the valve heaters have warmed up, have been installed.

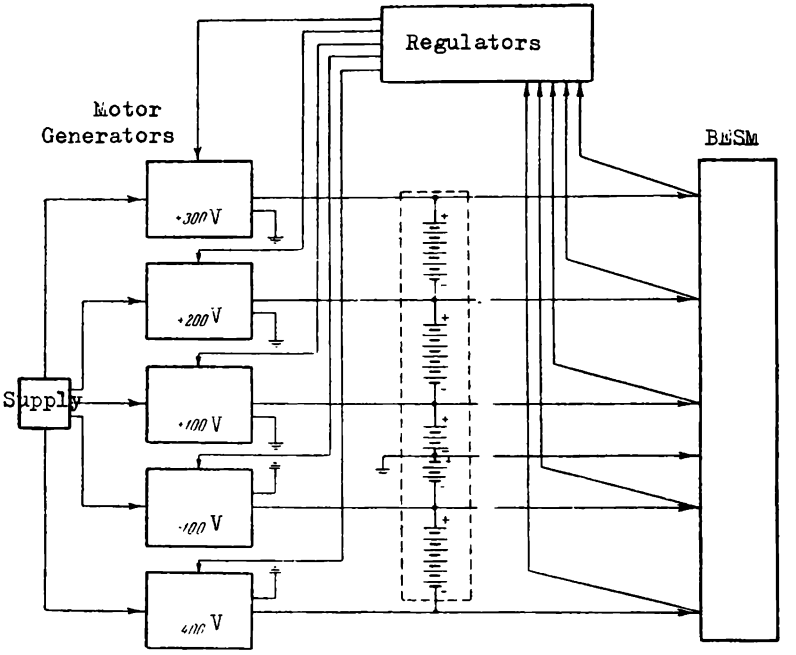

Fig. 10. Block diagram of the central power supply.

Thus, to secure reliable operation, the following demands are made on the d.c. power supplies:

a) Stability not worse than ±2% for standard elements, and not worse than ±0.1% for the main elements of the high-speed store VZU.

b) Impossibility of switching on the d.c. voltages without switching on the valve heaters.

c) Impossibility of switching on only some of the d.c. voltages.

One of the peculiarities of a d.c. power supply for electronic computers is the large number of voltage ratings, which lessens the reliability of working of the machine for a number of reasons.

(1) With a large variety of individual voltage values it is very hard to attain high stability of the whole power supply system, since, with an inconsiderable departure from the rating of individual voltages, the total departure of the power supply voltages can attain considerable size.

(2) A large number of make-before-break contacts oxidize during prolonged operation. This is an important factor which affects the reliability of working of the machine.

(3) With a large number of voltage values the whole power supply system becomes clumsy and complicated in operation.

During the whole course of operation of the machine, the number of individual ratings was reduced from 30 to 21.

Pulse disturbances and pulsation in the power supply lines cause dislocations of operation. For protection against these disturbances, d.c. motor generators working in parallel, with large filters, have been installed in the power supply system.

The machine operates by pulse codes, so the current requirements alter with a frequency between a few dozen c/s and about 1 Mc/s. To reduce the internal resistance of the d.c. power supplies to a minimum, trickle-charged storage batteries have been installed. These batteries could be replaced by large capacitive filters.

To improve reliability it is essential to carry out preventive checking regularly and strictly, with the object of detecting and removing defective valves; testing the departure from normal of the parameters of the radio-engineering components, and the state of the soldered joints and contacts; and checking the characteristics of the germanium diodes.

The following are the methods of preventive checking used for the machine:

a) operating the machine on set programmes;

b) supplying special voltages (-96 V; -98 V; -380 V; -420 V) to test the efficiency of flip-flops and inverters;

c) gradual lowering and raising of the heater voltage by ±7 to 12%;

d) gradual alteration of the basic voltages (-100 V; +100 V; +200 V) by ±3%.

In the course of prolonged working of BESM it was established that it is necessary and sufficient to carry out a preventive check once a day. Pulse induction and noise in the connecting circuits of individual elements have a great influence on the stability of operation, so the wiring was carried out with great care, and the sheaths of power cables and leads were earthed. The machine was earthed by means of copper strip 200 mm wide and 0.6 mm thick, welded to the framework of individual racks, which considerably reduced the ohmic and inductive resistance of the "earth" (Ref. 5).

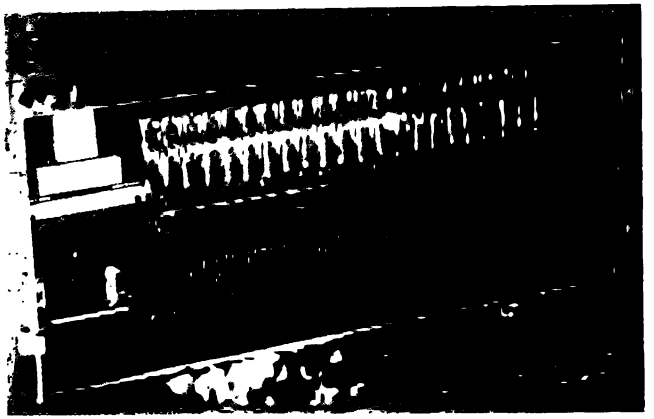

Fig. 11.

If the fuse in any section of a rack burns out, all d.c. voltages supplied to the rack in question are switched off. The fuses are installed in the input switchboards within the sections.

Fig. 11 shows such a switchboard. Besides fuses it contains an interlock relay and an indicating light. During operation of the machine it was established that the use of a safety device of this kind considerably lessens the reliability of the installations, since intermittences are caused by unreliable contacts between the insert and block of a fuse; therefore it is better to

replace the fuses by electromagnetic or thermal relays. Since voltages dangerous to the attendants (up to 1700 V) are used in the high-speed store, all doors of the cabinets in which high-voltage apparatus is installed have electrical

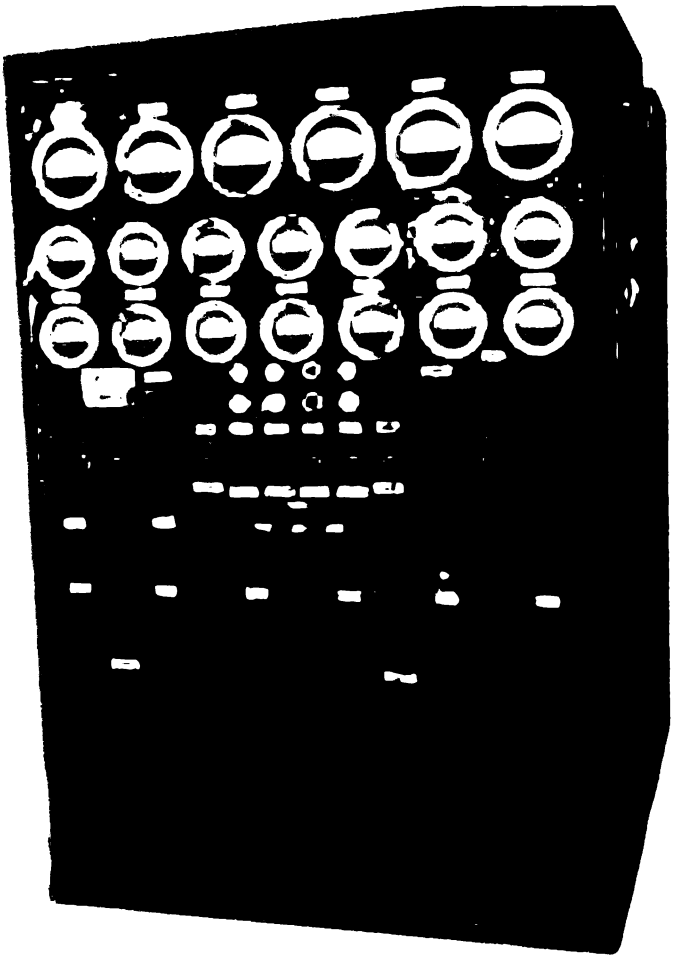

Fig. 12. Power supply rack.

interlock and mechanical dischargers. Links are installed near each supply panel in the racks; faulty panels are disconnected with their aid during adjustment of the machine. Similar links are installed in the input switchboards of the sections of the high speed store to cut off high voltages from a faulty section.

Visible and audible signals are used in the power supply system of the machine to facilitate the quick discovery and correction of faults, and also to give warning that high voltages are switched on.

All supervision, indication and protection devices (except the safety devices for elements of individual racks), devices for signalling, and also for control of power supply installations, are located in the power supply rack (Fig. 12).

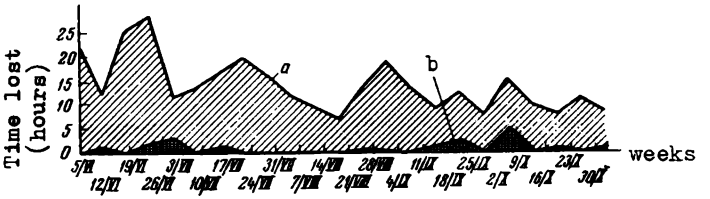

Fig. 13. a) total number of dislocations of the machine
b) dislocations of the machine due to the power supply system.

The number of dislocations of operation caused by bad functioning of the power supply installations is about 6% of all dislocations of the machine (see Fig. 13).

Preventive testing of the power supply installations occupies ten hours a month, which, with 24-hour operation of the machine, is less than 2% of the total machine time.

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VALVE TYPE NUMBERS

With the exceptions mentioned below, the valve type numbers quoted in this paper are American equivalents for the original types, and are as given in Russian-English Electronics and Physics Glossary, Consultants Bureau, New York (1957).

The type number 6J9 is a transliteration of the original number. The valve is a straight pentode with a 6.3 V indirectly-heated cathode. Its characteristics are not known.

The 6H5C (which is quoted in its original form) is a double triode in glass construction. Its characteristics, as given in the above-named publication, are: V_h 6.3 V, I_h 2.5 A, V_a 135 V, I_a 110 mA, R_k 250 Ω, g_m 6.7 mA/V, p_a 13 W per triode.

Editor

F. V. MAIOROV

DIGITAL INTEGRATING MACHINES (DIFFERENTIAL ANALYZERS)*

1. Introduction

The digital integrating machine, which is a device of the continuous-discrete type, might be called a digital analogue computer. This machine very successfully combines the continuous-action principle of solution of mathematical problems of analogue computers and the discrete counting methods of carrying out mathematical operations of digital computers. In contradistinction to "arithmetical" digital machines, in the digital integrating machine all mathematical operations are reduced to one integration operation, which can be carried out as an addition or subtraction of numbers. These operations are carried out by the digital integrator, which takes the place of the electromechanical or electronic integrator in analogue computers.

Since the machine includes a storage unit, the continuous solution of a mathematical problem can be carried out in sequence, one integration after another, by only one integration unit. In principle, just such a sequential method of solving a problem using only one integrator is possible in analogue computers, if they have a storage unit.

The combination of the principles of problem solution of analogue computers with digital methods permits the construction of a new type of digital machine, possessing the good qualities of both analogue computers and digital machines. On the one hand, the use of analogue computer methods of solving problems in digital integration machines makes it possible to attain continuous action, high operational speed, simplicity of adjustment, facility of

*Based on reading and theoretical investigations by the author.

introduction and formation of diverse functions, and easy operation of the machine. On the other hand, the use of a digital integration unit considerably improves the accuracy of calculations and flexibility and universality of the machine, simplifies its construction, and makes it more economical.

With a digital integrating machine there is no need for complicated, time-wasting programming of the problem, as there is with conventional digital machines. The machine can be switched quickly for the solution of different problems, and has great advantages over the conventional digital machine in flexibility of adjustment and operation.

The digital integrating machine was first developed in the U.S.A., in 1950, to solve differential equations in aerodynamics; it was given the name of "digital differential analyzer".

A machine of this type manufactured in the U.S.A., CRC-105, works with six-digit decimal numbers, and has a fairly high speed of calculation (3600 integrations a second with six-digit decimal numbers). It has a capacity of 60 integrators, each with 6 decimal digit places, while calculation is carried out with 12 decimal digits. The store is a magnetic drum with 12 tracks for the writing and reading of the codes of numbers and of programmes for connection of integrators.

Information input is on punched tape, on which various experimental functions can be encoded by 12 input channels. Results of calculation are recorded on punched tape for 12 channels. All information enters and is printed in the decimal system, but calculation in the machine is in the binary-decimal system. The machine contains about 400 valves.

Since 1950 various types of digital integrating machine have been developed in the U.S.A. for scientific and technical calculations, with 20, 60, 100 or more integrators.

They are used to solve sets of differential equations in aerodynamics describing flight trajectories, and also equations connected with research and calculations for rockets, guided missiles, submarines, etc. The power requirement of the machines is only 100 *W*, of which 75 *W** are required for the motor turning the drum.

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*For semiconductor diodes and triodes

Effective use of digital integrating machines for the control of real objects is secured by the high speed and continuity of calculation of the machines, and the simplicity of introducing external information.

Input parameters given as continuously-varying voltages and mechanical transpositions are converted, for integrating machines, into individual pulses applied serially to its input. Each pulse corresponds to a definite increment of a physical quantity, and the quantity itself can be represented at any moment as the sum of the pulses stored in the counter.

Thus the code of a number with which the machine is operating is formed as the sum of individual increments, which are represented (in a determinate scale) by pulses. The possibility of direct introduction of the code of a number as an integrand is not excluded.

The ability of an integrating machine to solve a problem by specified increments uninterruptedly, with a delay of not more than 0.001 to 0.01 sec, is a very valuable advantage. Indeed, since the machine works with increments of the quantities uninterruptedly supplied to its input, it is possible to attain a speed of calculation of up to 1000 solutions per second, or to get 1000 points of the required function per second.

Feeding of input data from various sources, and connexion of the machine with the controlled object, can be very easily realized, with great flexibility of connexions and with the possibility of switching them.

An integrating machine is essentially an automatic device in which automatic control of calculation is achieved by extensive use of feedback.

The advantages of digital integrating machines are:

1) Reliability of operation, because of the small number of electronic elements and the automatic principle of operation.

2) The automatic principle of operation, and use of feedback.

3) Simplicity of construction and compactness.

4) Flexibility of the control system and simplicity of switching for solutions of diverse problems.

5) High speed of calculation.

6) Accuracy, which is higher than in electromechanical devices.

7) No accumulation of errors in integration.

8) Uninterrupted output of calculated data.

9) Simplicity and flexibility of methods of obtaining input data from various sources.

10) Easy presentation and conversion of input data given as graphs, tables, instrument readings, etc.

11) Ease of operation.

12) Economy of production.

13) The small power supply required.

The disadvantages of digital integrating machines are:

1) Linear dependence of the degree of accuracy obtained on the time taken in solution. In consequence of this, accuracy of solution is in practice limited to 6 or 7 decimal places.

2) A certain amount of time is required for the processing of input (initial) data in the case of the control of objects, depending on the working speed of the machine and on the size of the discrepancy between the initial data and the initial conditions specified in the machine.

2. Block Diagram of an Integrating Machine

A digital integrating machine capable of the control of real objects consists of the basic units shown in Fig. 1.

1) The conversion unit (1) for conversion of input data supplied in continuous form (as voltages or as mechanical transpositions) by measuring instruments or other devices. The conversion unit realizes the multichannel conversion of input quantities a specified number of times per second.

2) The function unit (2) is used for the introduction of functions of one or several variables; functional dependences can be presented as graphs or tables. Individual functions can be written directly on punched tape in discrete form and fed into the machine by the function unit.

3) The operational storage unit (3) is connected

directly to the integrator. It stores the results of intermediate calculations during integration, input data converted to discrete form, coded calculation programmes, and initial conditions from the permanent store.

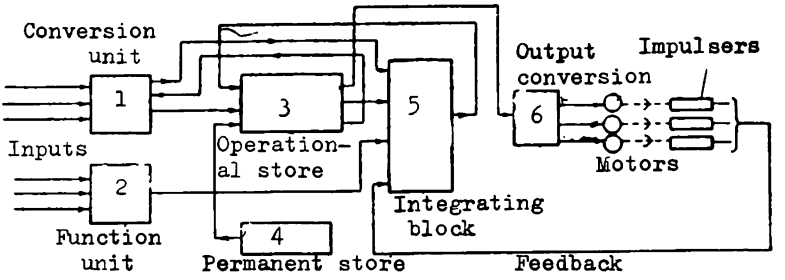

Fig. 1. Block diagram of a digital integrating machine.

4) The permanent store (4) consists of a punched tape or some other device on which are written in code form: (a) the sequence of connections of the integrators (that is, the calculation programme) and (b) the initial conditions for the solution of the problem. The permanent store can hold programmes and initial data for several different problems. Adjustment of the machine for the solution of a given problem is achieved by switching. Magnetic drums, ferrite core storage units, crystal diodes and triodes, capacitor storage units, etc., can be used both as operational and permanent stores. Ultrasonic delay lines (solid metal, quartz magnetostrictive) can be used only as an operational store.

5) The integrating block (5) carries out in sequence all the integration operations required for the solution of a problem. The sequence of operations is given by the coded programme in the operational store. The integration operation reduces to addition and subtraction of number codes held in the operational store. Multiplication and division, formation of functions, raising of powers, and other operations, are carried out by the integrators.

6) The operational store feeds initial data into the integrating block, and the intermediate results of

calculation are supplied to the operational store for temporary storage. Initial data, converted into numbers by the conversion block (6) are also stored in units of the operational store. When alteration of the initial data is required, the number code formerly stored in the operational store is replaced by a new code from the converter.

External information supplied to the integrating block from the function unit in discrete form is fed directly into the integrators, not passing through the operational store. This permits the amount of information fed into the machine to be increased without complicating the operational store. The final results of calculations in the integrating block can be written at the output in the form of number codes on punched tape, or of graphs of the functions required. For automatic control of a real object, it is necessary for the machine to compare the calculated value (A) of a controlled quantity with its controlled value (B).

The result of this comparison will be an error signal Δ A – B, which controls the external motor. This comparison of number codes (the subtraction A – B) is carried out in the computer itself, which presents the value of the discrepancy Δ in the form of a number code.

The output conversion unit converts the discrepancy Δ into a voltage for each of the output channels. Particular accuracy of conversion is not necessary, and it can be executed roughly, with an error of the order of several per cent. The discrepancy voltage is applied to the three motors, which control the quantities related to the object. The angular position of the shaft of each motor is measured by electromechanical counters or impulsers. The values of the controlled quantities are fed into the integrating block of the computer in the form of number codes or pulses. The feedback of the system controlled by the computer is connected to this block.

Controlled quantities, like input quantities, can be measured by the aid of some measuring instrument whose readings can be converted into discrete form by the conversion unit for input quantities. Feedback, in this case, will embrace all blocks of the computer.

3. The Integration Principle

In digital integrating machines the integral of any

function is approximately presented as the sum of the areas of simple rectangles, each of which corresponds to a specified increment Δx of the independent variable (Refs. 1, 3, 4).

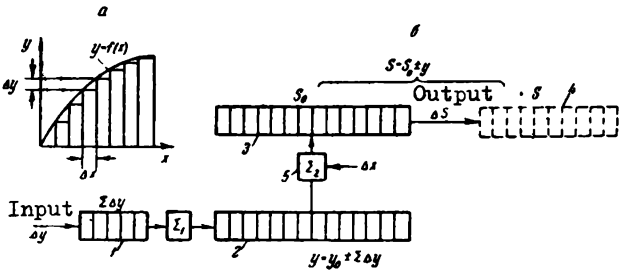

Fig. 2. Block diagram of a digital integrator.

Let us suppose that it is required to find the integrals of a given function $y = f(x)$. This integral is represented in Fig. 2 by the area bounded by the curve $y = f(x)$, and, by Euler's integration method, can be approximately represented by the sum of the areas of elementary rectangles. The current ordinate of y is the altitude of each rectangle, and the base is an increment Δx of the independent variable, which is divided into equal intervals for the whole range of variation of the variable x. Then the value of the integral S is:

$$S = \int_{x_0}^{x} y\,dx = \lim \sum_{i=1}^{i=n} y_i \Delta x_i + y_0 \approx \sum_{i-1}^{i-n} y_i \Delta x_i + x_0, \qquad (1)$$

where y_0 is the initial value of the function $y = f(x)$, and $\Delta x_i = x_{i+1} - x_i$ is an increment of the independent variable x.

We shall assume that the increment of the independent variable $\Delta x = 1$; that is, that every increment is taken as one unit of the count. Then

$$S \approx \sum_{i-1}^{i=m} y_i + y_0, \qquad (2)$$

That is, to calculate the value of the integral S it is sufficient to add all the ordinates corresponding to the

elementary rectangles. Thus the integration process is reduced to an addition of numbers representing the ordinates of y_i.

Each successive ordinate represents the previous ordinate plus (or minus) the increment Δ_{yi} of the ordinate for the interval $x_{i+1} - x_i = \Delta_{xi}$. So the value of the ordinate y_i can be calculated by adding to each previous value of the ordinate the increments of the ordinate Δ_y. Thus, for example,

$$\left.\begin{aligned} y_1 &= y_0 + \Delta y_1, \\ y_2 &= y_1 + \Delta y_2, \\ y_3 &= y_2 + \Delta y_3, \end{aligned}\right\} \tag{3}$$

$$y_n = y_{n-1} + \Delta y_n = y_0 + \Delta y_1 + \Delta y_2 + \ldots + \Delta y_n.$$

It can be seen from this that the current value of an ordinate y_i can be obtained by accumulating the increments of ordinates for all the preceding Δx sections.

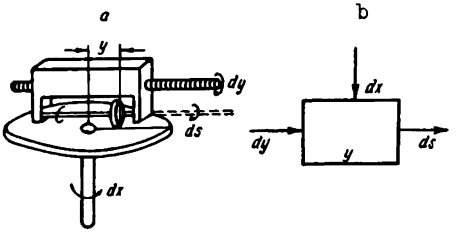

Fig. 3. Frictional integrator and digital integrator.

The digital integrator for calculation of the ordinates y_i and the values of the integral S, has two inputs and one output, as shown at (b) in Fig. 3. Increments of the integrand Δy are applied to the first input in the form of individual pulses. Increments of the independent variable Δx are applied to the second input.

The increment of the integral ΔS is obtained at the output of the integrator, also as individual pulses. To compare the digital integrator with a mechanical frictional

integrator, an increment of the integrand Δy corresponds to a unitary angular transposition of the screw (see Fig. 3a) which moves the carriage with the integrating roller. The value of the displacement y of the roller from the centre of the disc is obviously the sum of unitary angular transpositions, including its initial position; that is, it corresponds to the current ordinate of the curve $y = f(x)$. An increment Δx corresponds to a unitary angular rotation of the shaft of the disc, to which the integrating roller is functionally joined. This shaft represents the independent variable x. A unitary angular transposition ΔS of the shaft of the integrating roller represents an increment of the integral, since the full value of an angular transposition of the roller shaft, as we know, corresponds to the integral $S = \int y dx$. All three quantities, x, y, and S, are the sum of the elementary increments Δx, Δy, and ΔS accumulated at the corresponding input of the integrator.

The block diagram of a digital integrator can be presented as in Fig. 2. Let us suppose the increments Δx, Δy, ΔS to be given as individual pulses. At the Δy input of the integrator there is a reversible counter (1) which counts the pulses received. This enables us to supply pulses from several input channels to the input of the counter for each step of integration, and to reckon the number of pulses recorded by the counter as an increment of the integrand, defining this increment as the sum of certain elementary increments: that is, $\Sigma \Delta y$. This would correspond to the angular transposition of the screw y of the friction integrator, resulting from the simultaneous receipt through differential gears of angular increments from several input shafts.

The code, fixed by the counter 1, of the number $\Sigma \Delta y$, is summed at every step of the integration with the code of the number y_0, which is stored in the register (2) by the adder Σ_1. We get from this addition or subtraction a new value for the ordinate $y = y_0 \pm \Sigma \Delta y$ for each step of the integration.

At each step of the integration the code for y, stored in register 2, is transferred to register 3, which stores the number corresponding to the sum of the ordinates; that is, the value of the integral. The adder Σ_2 sums the code of y from register 2 and the code of S_0 from

register 3. Thus the adder carries out the operation

$$S = S_0 \pm y, \tag{4}$$

where S_0 is the code of the number stored in register 3, and corresponds to the initial value of the integral.

A summation is carried out every time an increment pulse of the independent variable x enters the Δx input of the integrator. Registers 2 and 3 have the same capacity, n binary digit places; that is, 2^n.

In adding two n-digit numbers on an increment signal Δx, register 3 may "overflow"; that is, an overflow pulse or carry pulse to a higher digit place may appear at the output. We shall reckon an overflow pulse of register 3 as an increment ΔS of the integral S at the integrator output. Increment pulses of the integral ΔS can accumulate in counter 4, shown in Fig. 2 by dotted lines. Register 3 and counter 4 can be considered as one counter with 2n digit places and divided in two parts. The first part, the register 3, stores the lower digits (the remainder, or "tail", of the number) of the integral S, and the counter 4 holds the left-hand digits of S from the $n + 1^{th}$ to the $2n^{th}$ digit. With this presentation of the integral S, it is registered by a counter having twice the number of digit places of the integrand register.

For instance, let x vary from 0 to 1 000 000 with an interval $\Delta x = 1$, and let the integrand $y = y_0 = 1\ 000\ 000$ =const maintain a constant value. For each summation of y and S we obtain one overflow pulse. The sum total of all the overflow pulses accumulated in the left-hand digit places of register 4 will be 1 000 000. Obviously the value of the integral is $1\ 000\ 000^2$.

The accumulation of overflow pulses ΔS supplied from the output of the integrator to register 4 is also an integration process. In the general case we can write for the increment ΔS of the integral

$$\Delta S = k \cdot y \cdot \Delta x, \tag{5}$$

where k is a constant multiplier equal to

$$k = \frac{1}{2^n} \tag{6}$$

for binary numbers, and n is the full number of digit

places of the counter-registers y and S, where S_0 denotes a number in register 3 of the counter (the remainder of the integral).

The coefficient k is the scale coefficient of the digital integrator. It shows that to get one overflow pulse at the output of the S register when $y = 1$ and $\Delta x = 1$ we must carry out 2^n summations, or 2^n steps, so that we get an overflow pulse ΔS at the output of register 3. If $y = 2^n$ (the full capacity of the integrand register 2) and $\Delta x = 1$, we shall get an overflow pulse at each step of the integration. With a machine presenting numbers in decimal form the coefficient k is

$$k = \frac{1}{10^n}, \tag{7}$$

where n is the number of decimal digit places in the register.

Passing from the increments Δx, Δy, ΔS to the derivatives characterizing the speed of change in time of x, y, S, we can write formula (1) as

$$\frac{ds}{dt} = k \cdot y \cdot \frac{dx}{dt} = k\left(\int \frac{dy}{dt} \cdot dt\right)\frac{dx}{dt} \tag{8}$$

or in the form of the integral

$$S = k\int y\,dx. \tag{9}$$

In digital integrating machines the value of the integral S is approximate, in consequence of errors arising from the following causes:

1) The approximate representation of the integral as the sum of the areas of rectangles. There is always some degree of error because of this. The greater the number of rectangles (and steps of integration) the nearer the sum of the areas of the rectangles approaches the value of the integral in formula (1). We can, by selecting the value of Δx and the number n of steps of integration, achieve an error less than a given value, that is,

$$\int_{x_0}^{x} y\,dx - \sum_{i=1}^{i=n} y_i (x_{i+1} - x_i) < \varepsilon. \tag{10}$$

2) The limited capacity of the register-counters y and S leads to the rounding-off of the result of calculations. To increase the degree of accuracy, calculation of the sum of ordinates is carried out in the digital integrating

machine with a double number of digit places; that is the value of the integral S is recorded by the two registers 3 and 4, which together have 2n digit places.

3) Binary coding of overflow pulses can, as we show below, be the cause of an error in calculating the integral of one unit in the lowest digit place of register 2 or 4. This error cannot accumulate in the course of calculation. It can be eliminated by using the so-called ternary method of coding overflow and increment pulses, in which an increment corresponds to +1, a negative increment to -1, and the absence of increment to 0.

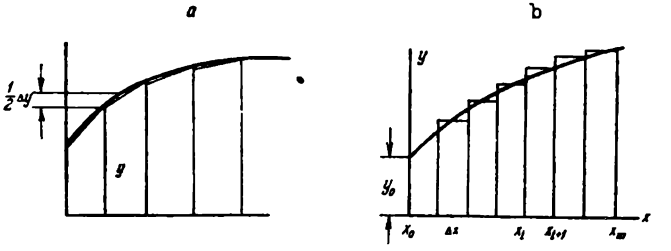

Fig. 4. Integration by trapezium.

However, the coding of three possible values for increments of a quantity complicates the construction of the machine. The error in integration by rectangles can also be diminished if we use the trapezium method illustrated by Fig. 4a, in which the curve y = f(x) approximates to a chord in each interval Δx. This method is equivalent to adding, with excess and deficiency, the areas of the rectangles shown in Fig. 4b, which have in each interval a mean ordinate which we can take as approximately equal to

$$y_0 + \tfrac{1}{2}\Delta y.$$

The increment of the integral (the area of the elementary rectangle) is in this case:

$$\Delta S = \left(y + \tfrac{1}{2}\Delta y\right) \cdot \Delta x. \qquad (11)$$

As is well known*, the trapezium method permits a reduction of the error of integration in formula (10) by about

*See V.I. Smirnov, A course of mathematical analysis, Part II, Gostekhizdat (1955).

ten times in comparison with Euler's rectangle method.

However, the trapezium method is recommended only in cases when the remaining errors are sufficiently small. With binary coding of the increments Δx, Δy, ΔS, when an increment can be either positive (+1) or negative (-1), and zero is represented as the sum of +1 and -1, the error of integration can be unity in the lowest digit place of the y and S registers, which is considerably greater than in the method of approximation of the sum of rectangles to the integral. So the use of the trapezium method is only justified if at the same time we use the ternary method of presentation of the increments Δx, Δy, and ΔS.

4. Systems of Coding Numbers

Operations in digital integrating machines are carried out with numbers with a fixed decimal point, varying in the range +1 to -1, and having a fractional part after the decimal point. All quantities fed in, on which operations are to be carried out, are expressed in a determinate scale as numbers varying within the limits of +1 and -1. Numbers are represented by a determinate number of binary or decimal digits, depending on the capacity of the registers of the integrator. For instance, if the register can hold a six-digit decimal number, the fractional part of the number contains six decimal figures.

The binary system is more suitable for coding numbers in the machine. In this system, which is illustrated by Fig. 5, the maximum positive number 0.99999 corresponds to |1| 111...11 in the binary system. The rectangle shows the code of the sign of the number. Positive numbers have code 1 in the sign cell, and negative numbers have code 0. The maximum negative number - 1 corresponds in binary code to |0| 000...00.

Table 1 shows the codes of some numbers in the accepted binary system.

We should remark that adding one unitary pulse in the lowest digit place to the maximum positive number value |1| 1111...11 turns it into |0| 000 ...00, that is, the maximum negative number. This is equivalent to an overflow of the y register.

The coding system described (Refs. 1, 5) is used only for the y and S registers. In the $\Sigma\Delta y$ counter and

register, we use the usual coding system for adding increment pulses of the ordinates Δy, in which '0' denotes the positive sign and '1' the negative. In this case the codes of numbers are held in the $\Sigma \Delta y$ counter and register in the form shown in Table 2 for three binary digits.

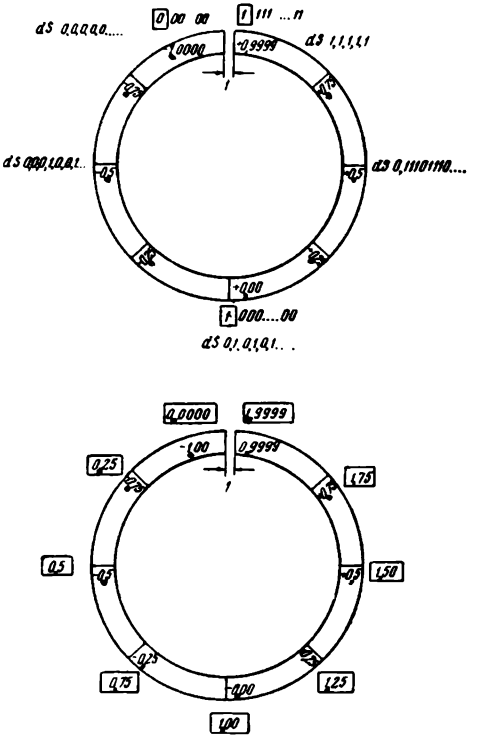

Fig. 5. Number coding system.

The correct result is obtained in adding or subtracting the coded numbers $\Sigma \Delta y$ and y. For instance:

Decimal system	Binary system
$y = +4$	0 000...00100
$+ \quad \Sigma\Delta y = -2$	$+$ 1 111...11110
$y + \Sigma\Delta y = +2$	1 000...00010

TABLE 1

Coding of numbers in the registers

Decimal No.	Binary Code	Decimal No.	Binary Code
+8	1 000...001000	—8	0 111...11000
+7	1 000...000111	—7	0 111...11001
+6	1 000...000110	—6	0 111...11010
+5	1 000...000101	—5	0 111...11011
+4	1 000...000100	—4	0 111...11100
+3	1 000...000011	—3	0 111...11101
+2	1 000...000010	—2	0 111...11110
+1	1 000...000001	—1	0 111...11111
+0	1 000...000000		

The coding system described has one important property which will be utilized later (section 9) in finding the layout of the so-called tracking integrator. It is that adding one unit to the lowest order digit of the maximum positive number y 1 111...11 turns it into the maximum negative number; that is,

TABLE 2

Number	Binary code	Number	Binary code
+4	0 100	—1	1 111
+3	0 011	—2	1 110
+2	0 010	—3	1 101
+1	0 001	—4	1 100
+0	0 000	—5	1 011

$$\begin{array}{rl} & \boxed{1}\ 111\ldots111 \\ + & \\ & \boxed{0}\ 000\ldots001 \\ \hline & \boxed{0}\ 000\ldots000 \end{array}$$

On the other hand, subtracting unity from the maximum negative value $y = \boxed{0}\ 000\ldots00$ turns it into the maximum positive number. In fact,

$$\begin{array}{rl} y \rightarrow & \boxed{0}\ 000\ldots000 \\ \Sigma\Delta y = -1 \rightarrow & \boxed{1}\ 111\ldots111 \\ \hline & \boxed{1}\ 111\ldots111 \end{array}$$

In integrating machines intended for technical calculations and for processing experimental data, all information is fed into the machine in the decimal system, which is convenient for checking. Results of calculation are also given in the decimal system. To avoid having to use complicated devices to convert binary codes into numbers in the decimal system, all calculations are also carried out in the decimal system (or, more precisely, in the binary-decimal system).

In this system numbers ranging between + 0.999...99 and −1.0000...00 (see Fig. 5) are encoded in the machine in the decimal system as the corresponding numbers ranging between 1.999...99 and 0.000...00. Thus positive numbers have code 1 before the point, and negative numbers have code 0. Positive numbers range between 1.9999 and 1.0000, and negative numbers between 0.0000 and 0.9999.

We should observe that negative numbers are shown as the decimal complement of 1.000...00. Thus, for instance, + 0.6321 will be presented in the machine as 1.6321, but the negative number − 0.6321 is encoded as 0.3679; that is, the part after the decimal point is the complement of 1.0000.

One negative unit in the lowest digit place of a four-figure decimal number is written in the machine as 0.9999, while +1 in the lowest digit place will be 1.0001. Summing the codes of y and $\Sigma\Delta y$ in the y register is carried out by the decimal system as well as by the binary system. The code of $\Sigma\Delta y$ can vary from 0 to 9 in the lowest digit place of a decimal counter for Δy increment pulses. The sign code of a number in the $\Sigma\Delta y$ counter

is the reverse of that in the y and S registers. Thus +1 in the lowest digit place of the $\Sigma\Delta y$ counter is registered as $\boxed{0}0001$, and -1 as $\boxed{1}9999$; -2 is written as 1.9998, and so on..

For example, let us add the numbers

$$\begin{array}{r} y=-2 \\ +\ \Sigma\Delta y=+4 \\ \hline y+\Sigma\Delta y=+2 \end{array}$$

or,in the decimal coding system,

$$\begin{array}{r} 1.0004 \\ 1.9998 \\ \hline 1.0002 \end{array}$$

that is, the number +2.

5. Integration Operations

As we explained in section (2), the process of integration in a digital integrating machine reduces to two summation operations for each step of the integration:

1) Summation of the code of the increments or sum of the increments $\Sigma\Delta y$ with the value already known for the integrand y_0; i.e., to obtaining the new value:

$$y = y_0 \pm \sum \Delta y. \tag{12}$$

2) Summation of the ordinates (the accumulation of values of the integral S), consisting of the summation of the new value of the integrand y and the previously-stored value of the integral S_0, i.e.

$$S = S_0 \pm y. \tag{13}$$

The first operation has been examined in detail in section (3). (See Refs. 1, 3, 4). Let us now consider the second integration operation.

The numbers S_0 and S in registers 3 and 4 are coded like the number y in register 2, with the difference that S_0 has another left-hand digit place after the sign cell, which can contain either code 0 or code 1, while in the y

register code 0 always stands in this digit place. The code in the left-hand digit place of S_0 is selected in accordance with the operation (addition or subtraction) to be carried out with overflow (increment) ΔS at the output of the integrator. If the output of the integrator does not change sign (i.e., the increment ΔS must be further added to other increments at the input of the next integrator) we have code 0 after the sign digit. If the sign of ΔS changes, code 1 is selected.

For instance the code of $S_0 = +13$ is recorded thus:

$$\boxed{0}\,|\underline{1}|\,000\ldots001101,$$

where code 0 is shown in the overflow position $\boxed{\ }$.

With change of sign of ΔS to the opposite ($-\Delta S$) the code of $+13$ in the S_0 register is written with code 1 in the overflow position, i.e.,

$$\boxed{1}\,|\underline{1}|\,000\ldots001101.$$

It is easy to see that in this case the code of the overflow pulse changes to its opposite. For instance, in adding $S_0 = +13$ to $y = +7$, we get in the first case

$$\begin{array}{rl} S_0 \rightarrow & \boxed{0}\,|\underline{1}|\,000\ldots001101 \\ y \rightarrow & \boxed{0}\,|\underline{1}|\,000\ldots000111 \\ \hline \text{overflow pulse code} \quad \leftarrow & \boxed{1}\,|\underline{0}|\,000\ldots010100 \end{array}$$

In the second case:

$$\begin{array}{rl} & |\underline{1}|\,|\underline{1}|\,00\ldots001101 \\ & \boxed{0}\,|\underline{1}|\,00\ldots000111 \\ \hline \text{overflow pulse}_0 \text{ code} \quad \leftarrow & \boxed{0}\,|\underline{0}|\,00\ldots010100 \end{array}$$

In integrating machines the increments ΔS, Δy and Δx are usually coded in the binary system, as it is simplest to write in the store only the two states 1 and 0. Code 1 corresponds to the presence of an overflow or increment pulse, signifying a positive increment equal to $+1$. Code 0 corresponds to the absence of an overflow pulse, and is decoded in the machine as an increment of -1.

The absence of an increment or zero at the output of the integrator corresponds to the series of overflow pulse codes 010101...01, which corresponds to +1, −1, +1, −1, and so on, i.e., to a zero integral increment.

We shall illustrate by some examples the process of addition and subtraction of the numbers S_0 and y for every step of the integration, and we shall establish when overflow pulses corresponding to an increment of the integral are supplied to the output of the integrator from register 3.

Example 1. Let us suppose that the initial value of the integral $S_0 = 0$, and that the integrand y has the code $\overline{1}|000...001$, i.e., has unity in the lowest digit place, and maintains a constant value during integration (y = const). Then, at each step of the integration, when y and S_0 are added, unity will be added to register S_0.

At the first step

$$\begin{array}{rl} S_0 \rightarrow & \overline{|1|}\ 0000...00 \\ + & \\ y_0 \rightarrow & \overline{|1|}\ 000\ ...01 \\ \hline \text{overflow pulse code } 1 \leftarrow & \overline{|0|}\ 000\ ...01 \end{array}$$

At the second step

$$\begin{array}{rl} S_0 \rightarrow & \overline{|0|}\ 00....01 \\ + & \\ y_0 \rightarrow & \overline{|1|}\ 00....01 \\ \hline \text{overflow pulse code } 0 \leftarrow & \overline{|1|}\ 00...010 \text{ etc.} \end{array}$$

In this way the series of overflow pulses 1,0,1,0, etc. is supplied to the output of the integrator; this corresponds to an increment of the integral of +1, −1, +1, −1, etc., i.e., to zero.

This series of overflow pulses continues until unity appears in the highest digit place of the code of the number in the S_0 register, which will happen after 2^n additions.

So we see that if we alternately add to and subtract from the initial value of the integral S_0 one and the same number y (i.e., the function changes sign, and the increment

of the integral is zero) we get the sequence of overflow pulses 1,0,1,0, etc., at the output of the integrator.

Example 2. Let us suppose that y is equal to the maximum positive number |1| 111...11, and maintains its value, and that S_0 is equal to zero.

Then at each step of the integration we get:

$S_0 \rightarrow$ |1| 00....00
\+
$y_0 \rightarrow$ |1| 11....11

overflow pulse code $1 \leftarrow$ |0| 11....11

At the second step of integration

$S_0 \rightarrow$ |0| 11...11
\+
$y \rightarrow$ |1| 11...11

overflow pulse code $1 \rightarrow$ |0| 11...10 etc.

i.e., to the maximum positive value of the integrand, there corresponds the series of overflow pulse codes 1, 1, 1, 1 etc.

In the same way we learn that to the maximum negative value of the integrand y = 0.000...00, there corresponds a series of overflow pulse codes 0,0,0,0 etc., which is decoded in the machine as a sequence of negative increments -1, -1, -1, -1, etc. Since the sequence of overflow pulses at the output of the integrator characterizes the speed of growth of the value of the integral stored in register 4 of the system shown in Fig. 2, we can say that there corresponds to the maximum positive value of the integrand y the maximum speed of growth of the integral, or the maximum positive speed of overflows characterized by the overflow code sequence 1,1,1,1, etc. at the integrator output.

To the maximum negative value of the integrand corresponds a maximum speed of overflows characterized by the code sequence 0,0,0,0,0 (-1, -1, etc.) at the output.

When the integrand has a zero value (i.e., the code |1|000...00), there corresponds to this value a zero speed of increment of the integral, i.e., the sequence of overflow pulse codes 1,0,1,0,1,0, etc. Interpreting these data, we come to the following conclusion: to a constant

speed of growth of increments of the integral there corresponds the value of the integrand, if it maintains a constant value. To a variable value of the integrand there corresponds a variable speed of growth of the increments (or overflows) at the output of the integrator. We can easily see this from two examples.

Example 3. The value of the integrand in the decimal coding system is y = 0.5, i.e., half the maximum negative value. Adding y and S_0 in the decimal coding system, we obtain:

a) at the first step

	S_0 0.0
	+
	y 0.5
overflow pulse code	0 ← 0.5 sum

b) at the second step

	$S_0 \rightarrow$ 0.5
	+
	$y \rightarrow$ 0.5
overflow pulse code	0 ← 1.0 sum

c) at the third step

	$S_0 \rightarrow$ 1.0
	+
	$y \rightarrow$ 0.5
overflow pulse code	0 ← 1.5

d) at the fourth step

	$S_0 \rightarrow$ 1.5
	+
	$y \rightarrow$ 0.5
overflow pulse code	1 ← 0.0 etc.

It is clear from this that when y = 0.5 (in the decimal coding system) the sequence of overflow pulse codes at the output of the integrator is 0,0,0,1,0,0,0,1 etc. This corresponds to half the maximum negative speed of growth of increments of the integral. In fact, the maximum negative speed of increments is represented by four negative increments for four steps of integration. In this example

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we have only two negative increments $1, -1, -1, -1 = 2(-1)$.

The results obtained are shown in Table 3.

TABLE 3

Code sequences of overflow pulses at the output of an integrator for eight steps of integration.

Value of y in the decimal coding system	Sequence of overflow codes		Sum of increments for 8 steps of integration	Binary code
$y = 0$	codes	0 0 0 0 0 0 0 0	-8	$\overline{0}$ 00...00 maximum negative value
	equivalent increment	$-1-1-1-1-1-1-1-1$		
$y = 0{,}5$	codes	0 0 0 0 0 0 0 0	-4	
	equivalent increment	$-1-1-1+1-1-1-1+1$		
$y = 1{,}0$	codes	0 0 0 1 0 0 0 1	0	$\overline{1}$ 000...00 zero
	equivalent increment	$-1+1-1+1-1+1-1+1$		
$y = 1{,}5$	codes	0 1 0 1 0 1 0 1	$+4$	—
	equivalent increment	$-1+1+1+1-1+1+1+1$		
$y = 1{,}9999$	codes	0 1 1 1 0 1 1 1	$+8$	$\overline{1}$ 1111...11 maximum positive value
	equivalent increment	$+1+1+1+1+1+1+1+1$		

Since overflow pulse codes have only two values (0 or 1), the accumulated sum of the increments of the integral can

differ from the true sum by +1 or -1.

For instance, if the increment ΔS is absent, +1 or -1 is received in the S register at each step of integration, which involves an error of +1 in the lowest digit for every odd step of the integration. This error, which fluctuates around zero, can be eliminated by using the ternary coding system, when the increments +1, 0, and -1 are represented by three different codes.

Summation of the ordinates $S_0 \pm y$ is carried out every time that a pulse of the increment Δx of the independent variable x is applied to the Δx input of the integrator. Only one pulse (one Δx increment) can be applied to this input for each step of the integration, while several pulses from different channels can be applied to the Δy input at every step. The codes of the Δx increment pulses have, like the codes for Δy and ΔS, two values, 1 and 0 ($\Delta x = -1$). With code 1 at the Δx input, the operation $S_0 + y$ takes place; with code 0 the operation is $S_0 - y$. A zero increment of the independent variable means the alternate addition and subtraction $S_0 \pm y$. In this case the value of the integral does not change. The system of coding the increments Δx, Δy, and ΔS described here makes interconnexion of them in any sequence possible. The output of an integrator can be applied to one of its own inputs, i.e., feedback can be realized.

6. The Magnetic Drum Serial Integrating Unit

In the description of the digital integrator it has been assumed that the y and S counter registers of each integrator consisted of electronic valves. This, however, would call for too much electronic equipment if there were several separate integrators.

As the machine has a store, we can carry out serial integration by one adder only, transferring to the store the codes of y and S and the overflow pulses from the integrator outputs.

Instead of storing the codes for y, S, and ΔS for the different integrators in registers, we can write them on the surface of a magnetic drum. In this case a specified sector of the magnetic drum corresponds to each integrator in the circuit for the solution of an equation. Let us suppose the reading and writing heads of the magnetic drum

to be diametrically opposite (Fig. 6). The initial data for each integrator are written on the surface of the drum in sectors 1', 2', 3' etc. These initial data

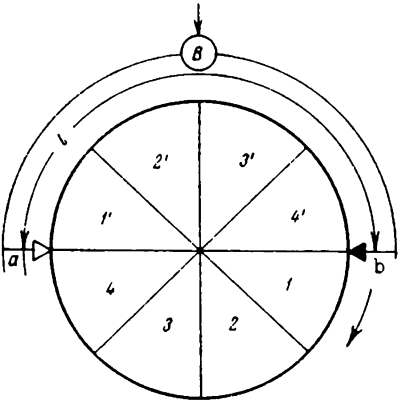

Fig. 6. Position of reading and writing heads with reference to magnetic drum.

are read by head (a) and sent to the adder. There are two parallel tracks on the drum, for simultaneous reading of the two numbers y and S. Almost simultaneously with the reading of the numbers, they are added serially, and the result of the calculation for each integrator is simultaneously recorded on the other half of the drum, in sectors 1, 2, 3 etc., by the head (b). Each step of the integration corresponds to a half-turn of the drum, and the codes written in a sector of the drum are replaced by new ones at every step, the previous record being erased. If the code of a number is to remain unchanged in the process of calculation, it is rewritten. To do this, the gate (B) in the circuit connecting the reading and writing heads opens, and the pulse codes read by head (a) in sector 1' are simultaneously written in sector 1. In the model we are considering, the possible number of integrators (sectors) is limited by the number of sectors in one half of the drum, i.e., it is determined by the length (L) of the arc between the heads (a) and (b).

The effective length L can be almost doubled if we

increase the distance between the reading and writing heads so far that writing and reading take place in adjoining sectors, or even in one and the same sector. The length of the arc of each sector is so selected that the whole of the code of a number can be written. One digit place at the beginning of each number is allocated for writing the so-called start pulse (SP), which controls the beginning of the calculation. One digit place at the end of the number is allocated to the change of sign of the overflow in the S_0 register. Thus the full code of the number has n+3 digit places, where n is the number of digits in the number itself. Writing of the codes of each digit is done at strictly fixed intervals, by the aid of a clock pulse. To synchronize reading and writing, a pulse sent to the reading or recording head is first stored by a trigger, which controls a gate, which admits or withholds pulses to the recording head. Since the clock pulses follow at fixed intervals, writing of number codes takes place at the same intervals.

If, for instance, the clock pulses follow at an interval of 0.2 mm, to write a number with 5 decimal places (16 binary places) the length of the arc of each sector must be $(16+3)0.2 = 3.8$ mm.

Fig. 7 shows the circuit of a digital integrating machine. Its principal element, acting as a number store, is the magnetic drum. In carrying out calculations it revolves at a constant speed (3,000 to 6,000 r.p.m.) in one direction. There are six parallel tracks on the surface of the drum. Each track has one reading and one writing head, except for the clock pulse track (CP) which has only a reading head. The S and y tracks serve for the writing of the codes of full digit place numbers of the integrand y and the integral S, corresponding to registers 2 and 3 in Fig. 2.

Increments of the integral ΔS, in the form of overflow pulses at the integrator output, are written on the special ΔS track.

Let us suppose the writing and reading heads on each of the four tracks y, S, Ax, Ay to be at an angle of 180° to one another. On the track for storing overflows of the integrators, ΔS, the writing and reading heads are separated by a distance a little less than the length of the arc of one sector, so that overflow pulses from all the integrators can be written and re-written within the

limits of one sector.* Besides the S, y, and ΔS tracks there are the tracks Ax, Ay, for writing the so-called address code Ax, Ay, by which interconnexion of the integrator outputs is brought about. Connexion is performed by readout of the required overflow pulse from

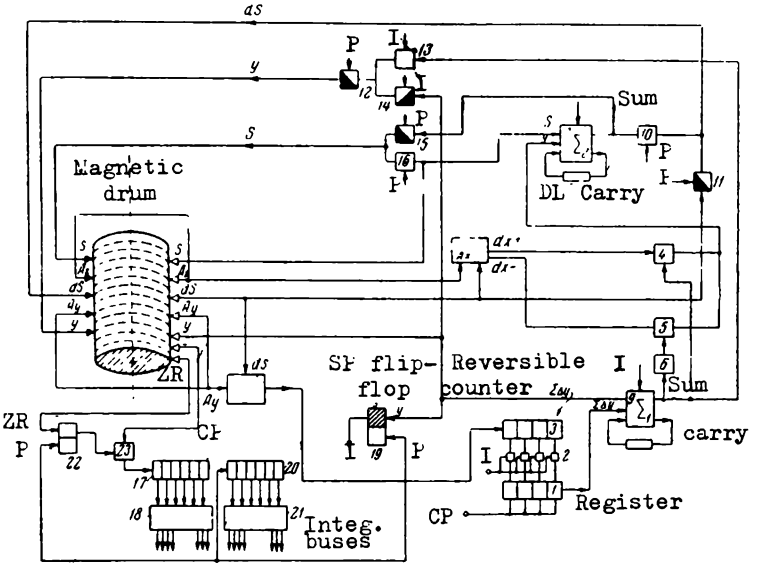

Fig. 7. Circuit diagram of a digital integrating machine.

track ΔS to the Δx or Δy input of each integrator. To do this, the various Ax and Ay codes are written on the Ax and Ay tracks on each sector of the magnetic drum, according to the equation to be solved. They remain unchanged throughout the solution of the problem, and are rewritten throughout on the other half of the drum, by means of the connexion between the reading and writing heads.

Each of the tracks y, S, Ax, and Ay acts in the manner of a delay line on the magnetic drum. The codes of the numbers recorded on these tracks circulate in them, in

*The writing of overflow pulses will be considered in detail below.

the form of a fixed sequence of pulses. Frequency of circulation is determined by the frequency of the clock pulses, which depends on the speed of rotation of the drum. The length L of the y, S, Ay, and Ax tracks is the same, and is an arc almost equal to the circumference of the drum. It includes all the sectors of the drum which are taking part in the calculation. The length of the ΔS overflow delay line is small, and is approximately equal to the arc of one sector of the drum. If, for instance, 60 sixteen-digit numbers are recorded on the surface of the drum for each of 60 integrators, and the speed of rotation of the drum is such that the clock pulses occur at intervals of 10 μsec, the length of a delay line L for the y, S, Ax, and Ay tracks will be 60 x 16 x 10 = 9600 μsec, and the length of the delay line for the ΔS track will be only 15 x 10 = 150μsec.

Delay lines on the magnetic drum can be completely replaced by delay lines of other types; by quartz magnetostriction types, for instance. In this case the principle of working of the integrating machine remains as before, but the operational speed can be considerably increased. The increased speed can be used to shorten the time taken in the solution of a problem, or to increase the extent of the problems to be solved.

Let us now consider the integration process, which, as we showed in section (2), consists of two operations of summation for each step of the integration:

$$1.\ y_0 \pm \Sigma\Delta y = y \quad (\text{adder } \Sigma_1);$$
$$2.\ S_0 \pm y = S \quad (\text{adder } \Sigma_2),$$

where (y_0, S_0) and (y, S) are the initial and terminal values of the integrand and the integral at each step. The integration process begins with the forming of the sum $\Sigma\Delta y$ by the summation of overflow pulses from the outputs of those integrators which, in accordance with the programme, must be connected to the Δy input of the given integrator. Thus the outputs of any number of preceding integrators can be applied to the Δy input of the given integrator, and the summation of the increments of individual integrators becomes possible.

The process of forming the sum $\Sigma\Delta y$ is displaced with respect to time by one sector, i.e., the summation of $\Sigma\Delta y$ takes place in the previous sector for the next integration sector, and so on. To this end the reading

and writing head ΔS is displaced one sector backwards, with reference to the reading heads y and S.

Overflow pulses recorded in this sector on the ΔS track are read by the ΔS head, and are fed to the dy or dx input of the integrator. Selection of the requisite overflow pulses ΔS for the Δy or Δx inputs is made by a coincidence circuit in the Ax or Ay block, in agreement with the address code of Ax or Ay.

As we shall show later, ΔS overflow pulses from all the integrators are written in each sector of the ΔS track in the order of their reference numbers. To connect the output of one integrator with any input of the following integrator, code 1 or 0 (presence or absence of a pulse) is written on the address tracks Ax and Ay. Each sector of the drum has its own particular sequence of Ax and Ay codes. By this means the output ΔS of any integrator can be fed to an input of a following integrator by selection with the aid of a coincidence circuit.

ΔS increments selected by the circuit of the Ay block are first summated in the reversible counter $\Sigma \Delta y$, which adds code 1 as an increment of +1, and code 0 as an increment of -1. Before the start of integration, the number registered in the counter is transferred to a shift register. Counter and register usually have 3 binary digit places and one sign place each, so increments from 7 different channels can be fed to the Δy input of an integrator. Shift of the coded number $\Sigma \Delta y$ and its transfer in the form of a series of pulses to the input of the adder Σ_1 are carried out by clock pulses supplied to the shift bus of the register.

Fig. 6 is a diagram of a three-digit-place counter $\Sigma \Delta y$ with a shift register. Here the code of each digit of the number $\Sigma \Delta y$ registered in the trigger circuits of the counter is transferred to the register for all digits in parallel by the gates B_1 to B_4. These gates form a coincidence circuit, and are controlled by the anode voltage of the trigger circuits.

In transferring a number from the counter to a register, a clock pulse is supplied to the gates B_1 to B_4 simultaneously at the start of the addition of $\Sigma \Delta y$ and y. After transfer of $\Sigma \Delta y$ to the register, the counter is cleared by sending a pulse to the counter-clearing bus. When $\Sigma \Delta y$ is transferred to the register, the trigger

circuit of the sign of the counter controls gate B_4 so that B_0 is closed when the number $\Sigma \Delta y$ in the counter is positive. For a negative $\Sigma \Delta y$, B_4 is open. When n

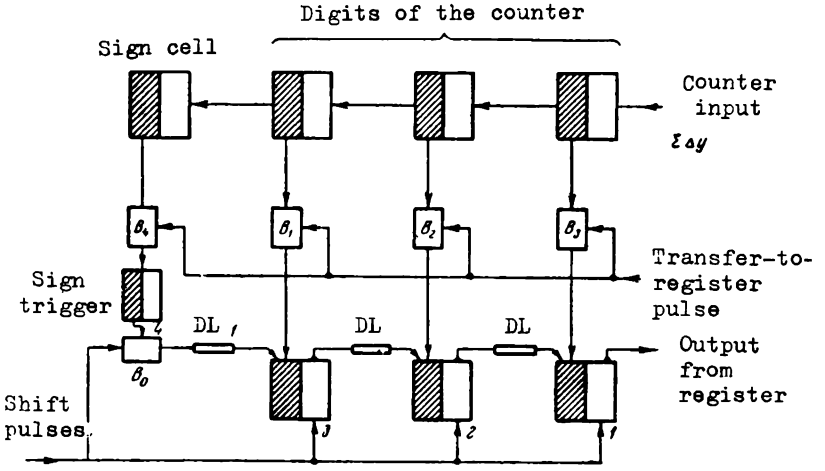

Fig. 8. Three-digit-place reversible counter.

clock pulses are fed to the shift busbar, the $\Sigma \Delta y$ register puts out the inverted code of $\Sigma \Delta y$ with a full number of digits corresponding to n digits of the number y, to which $\Sigma \Delta y$ is added. The delay line DL1 accumulates each shift pulse; and, after every pulse, cell 3 of the register is set in a position corresponding to code 1, if B_0 is open. This happens when there is a negative number in the counter.

For example, +6 and -6 in counter $\Sigma \Delta y$ are presented at the output of the register in the form:

$$+6 \text{ code } \overline{|0|} \quad 000\ldots00110$$

$$-6 \text{ code } \overline{|1|} \quad 111\ldots11010$$

Simultaneously with $\Sigma \Delta y$, the code of y, read from the y track of the magnetic drum, is fed to the adder input in the form of serial pulses. The single-digit-place adder Σ_1 adds or subtracts y and $\Sigma \Delta y$ serially, in

accordance with the sign of the counter $\Sigma\Delta y$. A positive y has code 1 in the sign cell, and is presented as direct code, but a negative number has code 0, and is presented in complementary code.

The result of the summation, in the form of a new value $y = y_0 \pm \Sigma\Delta y$, is supplied from the output of adder Σ_1 to the input of adder Σ_2 through gates 4 and 5 (Fig. 7). At the same time the output of adder Σ_1 is connected through gate 13 with the writing head of the magnetic drum for rewriting the initial (trigger) pulse in register y. The initial pulse SP acts as a signal for the start of summation in the adders. It can be previously written in any digit place of the y register. Its position is determined by the scales taken for $\Sigma\Delta y$ and y. If, for instance, the initial pulse is written in the third digit place of y, the lowest digit of $\Sigma\Delta y$ is added to the third digit of y; that is, there is a shift to the right by two digit places between the numbers to be added, in accordance with the specified scale.

The initial pulse written in the y register is fed to one of the inputs of flip-flop 19, and brings it into action. This flip-flop remains open during the application of the coded number by the reading head y. Only after the passing of pulse P, corresponding to the last code of the number y, does flip-flop 19 close.

The initial pulse from the output of flip-flop 19 controls gates 13 and 14. Gate 13 is a coincidence circuit which admits to the writing head all pulses from the output of adder Σ_1 with the exception of the initial one. Gate 14 is an anti-coincidence circuit, and admits only the initial pulse from channel y for rewriting.

The new value of y is fed serially from the output of adder Σ_1. It arrives at the input of adder Σ_2 simultaneously with the code of S_0 from the S reading head of the magnetic drum.

The circuit of block Ax, which selects overflow pulses for the address Ax, controls gates 4 and 5, through which the code of y passes to the adder Σ_2. Depending on code 1 or 0 at the output of the coincidence circuit, gate 4 or gate 5 opens. If the Δx increment has a positive value ($\Delta x +$), gate 4 opens, and the direct code of y is

fed to the input of adder Σ_2, i.e., the addition $S_0 + y$ takes place. If the Δx increment has a negative sign ($\Delta x -$), gate 5 opens, and the inverted code of y* is fed to the input of adder Σ_2, i.e., the subtraction $S_0 - y$ takes place. The result of the summation of S_0 and y is written on the S track of the magnetic drum. To do this the output of adder Σ_2 is connected across the anti-coincidence circuit 15 to the writing head of track S. This gate is open all the time, except at the moment when the last clock pulse P, corresponding to the last (highest) digit of S, passes. At this moment the highest digit of S is rewritten, by way of the open gate (coincidence circuit) 16.

The overflow pulse from the output of adder Σ_2, passing through the coincidence circuit 10 at the last clock pulse P, is written in the ΔS overflow pulse store line. Overflow pulses from all preceding integrators are re-written in the ΔS line through the anti-coincidence circuit 11, which is open only at the passing of the last clock pulse P of the given sector. The anti-coincidence gate 14 does not let the last digit of y through to the recording head, so the last digit of y is always 0.

All operations in the machine are controlled by clock pulses applied to the surface of the drum on the clock track (CP). The binary counter 17 counts these pulses. In order that any particular reading of this counter should always correspond to the same place on the drum, independently of the time of connecting the circuit, there is a track (ZR) to which one "zero reading pulse" is applied at a chosen spot on the surface of the drum. As soon as the zero reading pulse arrives at the ZR reading head, flip-flop 22 is triggered and gate 23 opens, admitting clock pulses to the counter. When the last clock pulse passes into the counter, flip-flop 22 reverts to its initial state. The clock pulse counter (of 4 or 5 binary digit places) is connected to a diode matrix, the decoder 18. At the output are 16 or more busbars,

*The inverse code for y is distinguished from the complementary code by one unit in the lowest digit place. It can be ignored in the code of S_0, since register 5 registers the remainder (lowest digits) of the number S_0.

each corresponding to a particular clock pulse, according to the address code of the numbers in registers y and S.

The integrator counter 20, with 5 or 6 binary digits, depending on the total number of integrators in the machine, counts the sectors of the magnetic drum (i.e., the integrators).

Pulses are supplied from the final bus of the decoder to the input of the integrator counter. Therefore, after the passing of each last pulse in the pulse counter, the counter reverts to the zero state. The integrator counter* has a diode matrix decoder with, say, 64 busbars at the output, corresponding to the numbers of the 64 integrators of the machine. The machine is controlled and the input and output circuits are connected by their aid. If the frequency of the clock pulses is 100 kc/s, switching of the buses at the output of the decoder also takes place at a frequency of 100 kc/s. Switching of the integrator buses (with 16 digit places in y and S) takes place at only 1/16th of this frequency; that is, at 6.25 kc/s.

7. Interconnection of Integrators. The ΔS Line

Overflow pulses from the ΔS outputs of different integrators are stored on the magnetic drum in the ΔS line. The length chosen for this line is less by one digit than the number of digits (codes) that can be recorded in one sector. Each sector of the drum can record n + 3 pulses, where n is the number of digit places in the code. One digit place is assigned to the sign cell, a second to the trigger pulse, and the last to the overflow pulse. In the ΔS line only n + 2 codes can be recorded. The overflow pulses written in the ΔS line are rewritten in all the remaining sectors of the magnetic drum. The reading and writing heads of the ΔS line are displaced relative to each other by one digit place; therefore when the overflow pulse codes are rewritten they are shifted by one digit place in each subsequent sector.

Let us suppose, for example, that a magnetic drum is divided into 6 sectors, and that we can write 6 digits in

*Shift registers or conversion circuits can be used instead of an integrator counter with decoders.

each of them, i.e., the maximum is 6 overflow pulse codes. Let us also suppose that the overflow pulse of each integrator is written in the last interval of each sector, at the points u_1, u_2, u_3, u_4, u_5, and u_6 (Fig. 9). This means that when the reading head is at point u_1 in sector 1, the overflow pulse code of the first integrator, shown by the figure 1, is recorded in the second sector. With the distance between the heads as shown, this pulse will be re-recorded in the third sector with its position

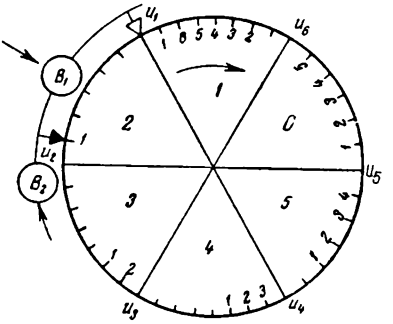

Fig. 9. The operation of an overflow line.

shifted by one digit place. In position u_2 of the reading head, a new overflow pulse of the second integrator (sector), shown by the figure 2, is recorded. As we see from Fig. 9, as the drum rotates, overflow pulses from the preceding integrators are recorded in each sector in a determined sequence, according to the order of the reference numbers of the integrators. In every succeeding sector the record of the overflow pulse from the preceding integrator is added to this record. When the drum completes a rotation, the new code of the overflow pulse of integrator 1 is recorded, instead of pulse 1 of the first integrator, in sector 1. In the second sector, the new value of the code of pulse 1 will be written, instead of its old value, in the same place as before, and so on.

For writing to be carried out in this way, it is essential that the gate B_1 should be closed only in the last interval (digit place) of each sector, i.e., at the points u_1, u_2...,

u_6. Gate B_2, through which the overflow pulse from the output of the integrator passes, must be open only at points $u_1 - u_6$. Since it must be possible to record the overflow pulses from all the integrators on each sector of the ΔS track, the number of integrators must not be greater than the number of digit places which can be written in each sector. Table 4 shows the writing of overflow pulses for the case in question with 6 integrators and 6 digit places in each sector.

TABLE 4

Order of digit place	Sectors									
	1	2	3	4	5	6	1	2	3	4
	1st rotation						2nd rotation			
(lowest)							2	3	4	5
2					1	2	3	4	5	6
3				1	2	3	4	5	6	1 new
4			1	2	3	4	5	6	1 new	2 new
5		1	2	3	4	5	6	1 new	2 new	3 new
6(last)	1	2	3	4	5	6	1 new	2 new	3 new	4 new

As we see from Table 4, at each rotation of the drum (second step of integration) the new values of the overflow pulses are written instead of the old (new 1, new 2, and so on).

In the circuit diagram (Fig. 7) the reading head of the ΔS track is connected to the writing head through gate 11, which plays the part of gate B_1 in the previous diagram. Gate 11 is an anti-coincidence circuit. It is open all the time for rewriting of overflow pulses, and closes only at the passing of the last clock pulse P in each sector. In this case the overflow pulse from the output of the integrator of adder Σ_2 is supplied to the writing head ΔS through gate 10, which is open only for the last pulse P.

The selection of overflow pulse codes from the number

of codes stored in the ΔS line is carried out by two selection circuits with addresses Ax and Ay. Interconnection of the integrators is made by the aid of these circuits, i.e., at each step of integration the overflow pulse ΔS of any preceding integrator is supplied to the Δx or Δy input of the succeeding integrator.

Let us examine the example of the selection of codes from the ΔS line to the Δy input of the succeeding integrator, in accord with code Ay written on the Ay track (Fig. 10).

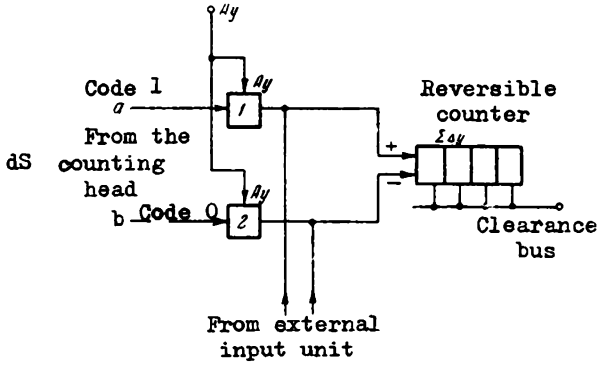

Fig. 10. Diagram of readout of overflow pulses at input of integrators (decoder Ay).

Code 1 or 0 obtained from the reading head of the ΔS line is transformed with the aid of a flip-flop into pulses on bus (a) or (b). Gates 1 and 2 admit these pulses to the cumulative counter $\Sigma \Delta y$ only when they coincide with pulses written on the Ay track as code 1. Pulses from bus (a) are supplied to the counter at the addition input, and from bus (b) at the subtraction input. Increment pulses of the integrand can be supplied from the external input units direct to the counter, as the diagram shows.

The circuit for readout of overflow pulses to the Δx input of the succeeding integrator with the address Ax is shown in Fig. 11. The read-out overflow pulse code stored in the ΔS line is first transferred by the flip-flop Fl, which has two separate inputs for code 1 and 0.

The code transferred by flip-flop Fl is transmitted, on

arrival of the initial pulse SI of the given integrator, to the inputs of flip-flop F2 through gates 3 and 4. Flip-flop F2 controls gates 5 and 6, through which the direct or inverse code of the number y passes from adder Σ_1 to adder Σ_2. The output of flip-flop F2, denoted by $\Delta x+$, corresponds to a positive increment, and $\Delta x-$ to a negative increment at the Δx input of the integrator. The inverse code of the number y is obtained from the direct code of this number by means of gate 7. When the code of the given digit of y is 1, this gate earths the clock pulses (CP) arriving at the input of the adder through gate 8, and almost all the voltage is dropped in the high resistance R. On the other hand, clock pulses corresponding to code 0 in the given digit place of y are supplied to the adder Σ_2, as gate 7 is closed. In this way we get the inverse code of y. The method described here can also be realized by using an anti-coincidence circuit for the clock pulses instead of gate 7.

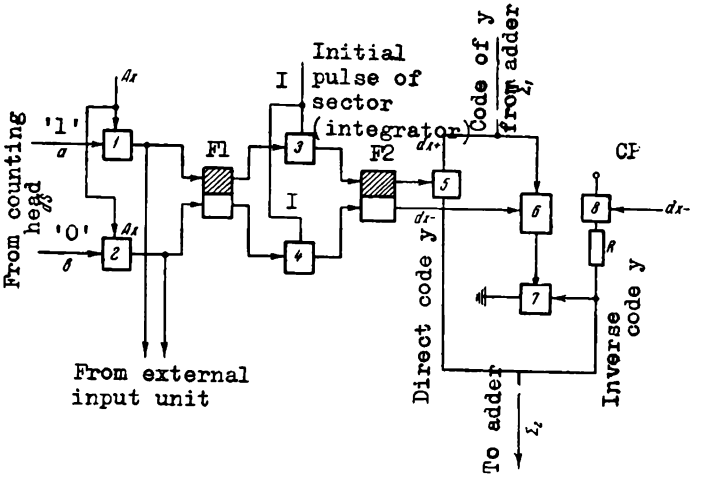

Fig. 11. Diagram of read-out of overflow pulses at inputs of integrators (decoder Ax).

So far we have supposed the number of integrators to be equal to or less than the number of digit places in one sector of the drum. If the number of integrators is greater than the number of digit places, which often

happens, such a simple method of writing overflows in the ΔS line is inapplicable. There are several methods of storing and reading out overflow pulses in the case of a great number of integrators.

One of these methods is based on the fact that most interconnections of integrators in the solving of a problem are made between integrators with reference numbers which are close together, and only a small number of connexions is required for integrators whose numbers are far apart.

The presence of one ΔS line having, say, a capacity of 16 binary digits, permits us to connect all the integrators from 1 to 16. If there are 32 integrators on the periphery of the drum, at one rotation (one step of integration) the first overflow pulses from integrators 1 to 16 will be written in the ΔS line in the first half-rotation of the drum, and then those from 17 to 32. As a result of the displacement of pulses in the ΔS line, in the second half-rotation the overflow pulse of the first integrator will be replaced by a pulse from the 17th integrator, the pulse of the second integrator by a pulse from the 18th, the pulse of the third by one from the 19th integrator, and so on. Thus it is always possible to connect integrators not more than 16 numbers apart, for instance, the 4th and 20th, 5th and 21st, and so on.

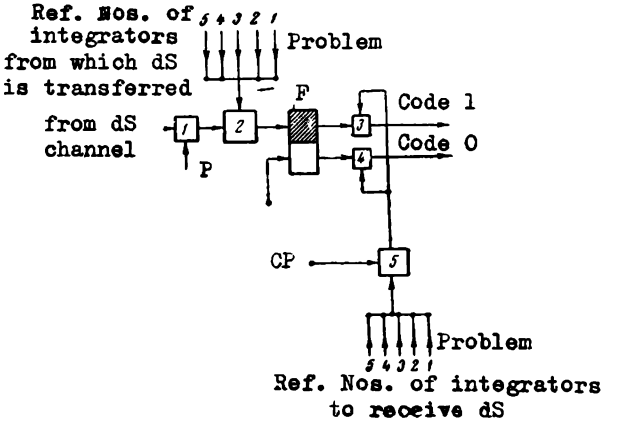

Fig. 12. Storage unit for overflow pulses.

If the programme requires interconnection of integrators more than 16 numbers apart, we can have a separate storage unit, as shown in Fig. 12.

A ΔS code which must be held for a longer time than the designed length of the overflow line is stored by the flip-flop unit 2. Gate 1 is opened by the last pulse in each sector, and gate 2 by the voltage of any one of the buses of the diode matrix of the integrators, corresponding to a given integrator. For the solution of problems, various integrator reference numbers may be required, as the diagram shows. The flip-flop F transfers the required ΔS pulse, and opens gate 3 or 4, depending on whether the code is 1 or 0. The ΔS code held in the flip-flop is read out with the aid of a clock pulse (CP) applied to gates 3 and 4. At the moment of coincidence of CP and the number of the integrator, a pulse is applied to the required integrator. Then gate 5 passes the clock pulse through to the $\Sigma\Delta y$ counter by way of the adding or subtracting bus, depending on the code of ΔS. After this the next clock pulse of the given sector returns the flip-flop to zero.

If it is necessary to store overflow pulses from several integrators set far apart from each other, a supplementary electromagnetic delay line DL can be used (Fig. 13). An

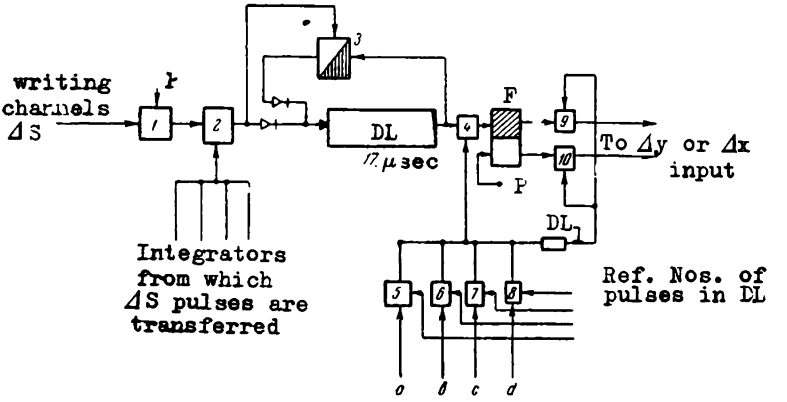

Fig. 13. Electromagnetic delay line for overflow pulses.

overflow pulse from the ΔS writing channel passing through gate 1 or 2 is stored in the delay line DL, and circulates

in it, because of feedback through gate 3. On the cessation of pulses from the ΔS channel, gate 3 closes and circulation of pulses in the line stops. The delay line DL has a length less by one digit place than the length corresponding to the full number of digit places in registers y and S of the integrator. In consequence of this, in circulation a shift of the position of the pulses in the line takes place, as in the ΔS line described above. A code is read out from DL through gate 4, which is controlled by one of the gates 5 to 8. In any integrator, the number of which is determined by the busbars a, b, c, d connected to the diode matrix of the integrator counter, one or several recorded pulses can be read out. Their number is determined by the number of gates 5 to 8. An overflow pulse code read out from DL is transferred by the flip-flop F and transmitted to the Δx or Δy input of the required integrator through gates 9 and 10. These gates are controlled by a pulse applied to the input of the flip-flop, which then opens gates 9 and 10, to which end the small delay line DL1 is included in the control circuit.*

A third method of storing and reading out overflow pulses of widely separated integrators consists of rewriting the codes for ΔS of the required integrator. This method can be used only if, for the solution of the problem, it is possible to allot sectors on the magnetic drum which are not occupied by calculations. Let us suppose that only 16 codes can be recorded in the ΔS line, and that the total number of sectors (integrators) is 32. Then, if we are required to connect the 1st integrator with the 30th, the free 16th integrator is assigned for the rewriting of the overflow pulse of the first integrator, and at its output the same overflow pulse code is obtained as in the first integrator. To this end the overflow pulse ΔS of the 1st integrator is supplied to the Δx input of the 16th integrator by writing the address Ax. As the integrand in the 16th integrator, the code of y (and S_0) $|\underline{1}|111\ldots$ is written. If the overflow pulse code Δx of the first integrator is 1, Δx will be positive for the 16th integrator, and vice versa.

In the first case, when $\Delta x = +1$, we get, as the result

*Flip-flop F can likewise be cleared by a pulse from gates 5 to 8 by way of the small delay line DL1.

of adding the codes:

y |1| 111...11

S_0 |1| 111...11

overflow pulse code |1| |1| 111...110,
ΔS is 1

i.e., the overflow pulse code of the 16th integrator is always 1.

In the second case, when $\Delta x = -1$, we get as the result of subtraction:

y |0| 000...00

S_0 |1| 111...11

overflow pulse code |0| |1| 111...11,
ΔS is 0

i.e., when the code for ΔS for the 1st integrator is 0, we always obtain 0 at the output of the 16th integrator.

The overflow pulse of the 16th integrator can be transferred to the 30th by aid of the ΔS line. In this way the 1st integrator can be connected to the 30th, and so on.

8. Introduction of Initial Conditions. Switching the Machine for the Solution of Various Problems

Before starting to solve a problem, we must introduce into the integrating machine the initial values of all integrands in the form of codes of numbers for the y registers. Besides this, the codes which determine the interconnection of the integrators must be written on the Ax and Ay tracks. Thus before solving a problem, coded information must be introduced into all sectors on the three tracks y, Ax, and Ay of the magnetic drum. As to the S and ΔS tracks, before the start of calculation all information must be erased from them, or must be written only as 0.

Switching the machine for the solution of various problems can be effected very simply, if we switch the information for the y, Ax, and Ay tracks from one channel to another. If we use a magnetic drum as the storage unit, the initial values and codes of the programmes of

different problems can be recorded on separate tracks of the drum (Fig. 14), from which they can be read out into the operational storage by the y, Ax, and Ay tracks when the problems to be solved are switched. This demands three supplementary amplifiers for the reading of this information. In solving a problem by the integration method, a certain amount of time is required initially for

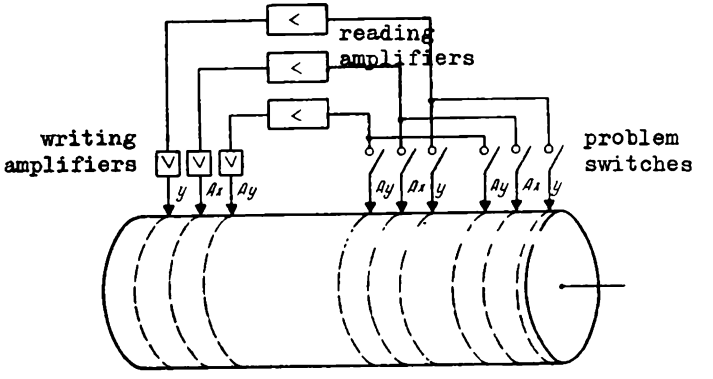

Fig. 14. Writing initial conditions on the tracks of a magnetic drum.

attaining the specified point on the curve to be integrated. This initial period or "working-in time", as it is called in computer terminology, can be shortened by selecting initial conditions lying as near as possible to the specified point. It is obvious that the working-in time can be halved if we select initial conditions for points lying in the centre of the given range of variation of the independent variables of the equation.

With a problem with a small number of independent variables, it is possible to shorten the time by 4 to 8 or more times, compared with the time required when initial conditions are given at the point of origin of the curve to be integrated.

Let us suppose that the problem to be solved is given in the form of an equation with three independent variables, x, y, z, i.e., we must calculate the value of the function

$$u = f(x, y, z), \tag{14}$$

given in the form of a determined mathematical dependence.

For each of the independent variables x, y, z we shall choose two points (x_1 and x_2, y_1 and y_2, z_1 and z_2) lying in the centres of the first and second halves of the possible range of variation of these variables (Fig. 15).

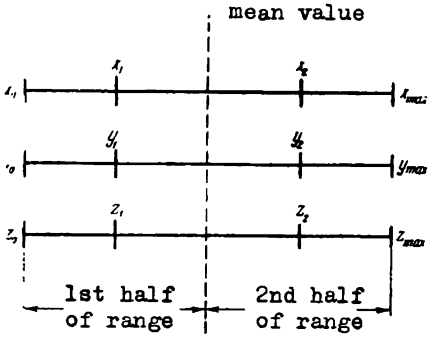

Fig. 15. Input of individual initial values, and switching.

If the selected point of the curve to be integrated lies in the first half of the range of variation of the variables x, y, z, on introducing the initial value of the function $u_1 = f(x, y, z)$ the working-in time of the solution will be four times smaller. This will also hold for the second half of the range, if we choose for the initial condition of the function the value

$$u_2 = f(x_2, y_2, z_2). \tag{15}$$

In the general case, for any values of the independent variables x, y, z the time can be shortened by four times if we introduce switching of the eight initial values depending on the values of x, y, and z. In fact, the number of possible combinations for three independent variables each having two values is $2^3 = 8$. Depending on which half of the range, first or second, contains the value of the independent variable x, y, or z, the following are the initial conditions of the function u which must be switched:

$$\left.\begin{aligned} u_1 &= f(x_1, y_1, z_1),\\ u_2 &= f(x_2, y_2, z_2),\\ u_3 &= f(x_1, y_1, z_2),\\ u_4 &= f(x_1, y_2, z_2),\\ u_5 &= f(x_2, y_2, z_1),\\ u_6 &= f(x_2, y_1, z_2),\\ u_7 &= f(x_1, y_2, z_1),\\ u_8 &= f(x_2, y_1, z_1). \end{aligned}\right\} \qquad (16)$$

Fig. 16 shows the switching of these initial conditions. The three relays have two positions, "off" and "on". For values of x, y, z lying in the first half of the range, these relays are off, while for the second half of the

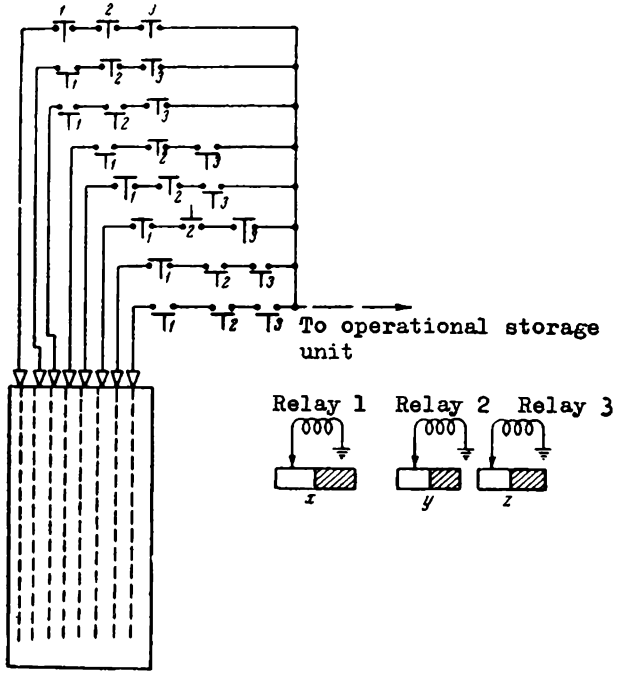

Fig. 16. Switching of initial conditions.

range they are on. Connexion and disconnexion of these relays can be brought about, for example, in accordance with the angular position of a shaft whose deflection is proportional to a measured quantity, or to the position of the highest digit in the binary counter registering the measured quantity, etc. The contacts of these relays form a kind of decoding circuit with eight switchable buses. In accordance with the state of the relay, these buses switch the initial conditions recorded on eight punched-tape tracks or on the magnetic drum. The initial conditions for all integrators by means of which equation (14) is solved must be written on each track. If the number of independent variables in the problem is increased, there is a rapid increase in the number of initial conditions required for shortening the working-in time by four. For instance, for four independent variables the number of initial conditions must be $2^4 = 16$, for five variables $2^5 = 32$, and so on.

To shorten the working-in time by 8 times, four fixed points for the whole range are required for each of the independent variables. The number of switchable initial conditions will in this case be:

for three independent variables $4^3 = 64$,

for four independent variables $4^4 = 256$.

Hence we see that decrease of the working-in time by more than four times demands a considerable increase in the number of elements of the decoding circuit.

9. The Following Integrator

By analogy with the following system, the following integrator serves as a kind of "zero apparatus" in the comparison of two or several numbers. The difference of two numbers $A - B = \Delta$ or the value of their mismatch (unbalance) is supplied to its Δy input. It can be supplied either as individual pulses, or as the sum of them, stored by the $\Sigma \Delta y$ counter as the value of the mismatch Δ.

At the dS integrator output we get, at each step of integration, a sequence of overflow pulses depending on the sign of Δ. If Δ is a positive number, we get the sequence 0,0,0,0,0, etc., until the value of the unbalance is zero. If Δ is a negative number, the sequence is

1,1,1, etc., until the value of the unbalance likewise becomes zero. If $\Delta = 0$, the sequence is 0,1,0,1,0,1,...

Thus at each step of the integration the following integrator generates at its output 1 or 0, depending on the sign of the unbalance Δ. The pulse codes generated are fed back to the input of the integrator. Since they are applied to the input of the $\Sigma\Delta y$ counter with the opposite sign to the pulse codes of the unbalance Δ by negative feedback, the value of the unbalance decreases with each step of the integration.

The operating principle of the following integrator is based on the fact that adding -1 to the greatest negative number 0.000...00 previously written in the y register converts it into the greatest positive number 1.111...11. On the other hand, adding +1 to the greatest positive number 1.111...11 converts it into the greatest negative number 0.000...00.

We shall explain the operation of the following integrator by examples.

Let us suppose the value of the unbalance supplied to the dy input of the integrator to be zero; that 0.00...000 has been previously written in the y and S registers; and that code 1 is supplied to the dx input at each step of the integration (for instance, the overflow pulse of the digit counter). Overflow pulses from the dS output of the

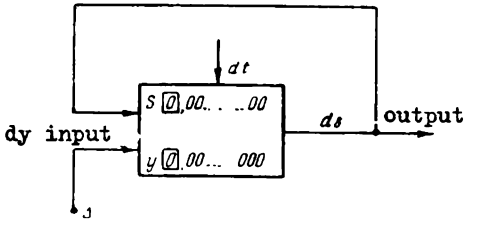

Fig. 17. Following integrator.

integrator are fed back to the input dy, as is shown in Fig. 17.

Then for each step of the integration we get the results shown in Table 5.

TABLE 5

Overflow pulses at the output of a following integrator with a zero value for the unbalance Δ at the input.

Step of integration	Increment	y register	S register	Sum S + y	Overflow pulse
1	—	[0] 00000	[0] 00000	[0] 00000	
				[0] 00000	
				[0] 00000	0
2	[1] 11111	[0] 00000	[0] 00000	[0] 00000	
		[1] 11111		[1] 11111	
		[1] 11111		[1] 11111	0
3	[1] 11111	[1] 11111	[1] 11111	[1] 11111	
		[1] 11111		[1] 11110	
		[1] 11110		[1] 11101	1
4	[0] 00001	[1] 11110	[1] 11101	[1] 11101	
		[0] 00001		[1] 11111	
		[1] 11111		[1] 11110	1
5	[0] 00001	[1] 11111	[1] 11100	[1] 11100	
		[0] 00001		[0] 00000	
		[0] 00000		[1] 11100	0
6	[1] 11111	[0] 00000	[1] 11100	[1] 11100	
		[1] 11111		[1] 11111	
		[1] 11111		[1] 11011	1
7	[0] 00001	[1] 11111	[0] 11011	[1] 11011	
		[0] 00001		[0] 00000	
		[0] 00000		[0] 11011	0
8	[1] 11111	[0] 00000		[1] 11011	
		[1] 11111		[1] 11111	
		[1] 11111		[1] 11010	1
				etc.	

It is obvious from this that after the initial triggering (first step of integration) the dS code sequence at the integrator output will be 0,1,0,1,0,1, etc.

Let us now suppose that $\Delta = 2$ (in the decimal system); then, writing the numbers in the decimal system, we get:

at the first step

$$\begin{array}{rl} & \boxed{0}\ 000\ S \\ + & \boxed{0}\ 002\ y \\ \hline \text{overflow pulse } dS\ \boxed{0} & \leftarrow \boxed{0}\ 002\ S \end{array}$$

at the second step

$$\begin{array}{rl} & \boxed{0}\ 002\ S \\ + & \boxed{0}\ 001\ y \\ \hline \text{overflow pulse } dS\ \boxed{0} & \leftarrow \boxed{0}\ 003\ S \end{array}$$

at the third step

$$\begin{array}{rl} & \boxed{0}\ 003\ S \\ + & \boxed{0}\ 000\ y \\ \hline \text{overflow pulse } dS\ \boxed{0} & \leftarrow \boxed{0}\ 003\ S \end{array}$$

at the fourth step

$$\begin{array}{rl} & \boxed{0}\ 003\ S \\ + & \boxed{1}\ 999\ y \\ \hline \text{overflow pulse } dS\ \boxed{1} & \leftarrow \boxed{0}\ 002\ S \end{array}$$

at the fifth step

$$\begin{array}{rl} & 0\ 002\ S \\ + & 0\ 000\ y \\ \hline \text{overflow pulse } dS\ \boxed{0} & \leftarrow 0\ 002\ S \end{array}$$

etc.

In this case, until zero speed of overflow pulses is attained we get at the integrator output two extra 0 codes, compensating the unbalance $\Delta = 2$ at the Δ y input; after which we get zero speed 0,1,0,1,0,1,0 etc. at the input.

The following integrator can be used for direct comparison of two quantities A - B = Δ if the increments dA

and dB are supplied by two channels to the dy input of the integrator (Fig. 18). Then the difference A - B will "finish itself off"at the dS output in the form of overflow pulses (with the opposite sign).

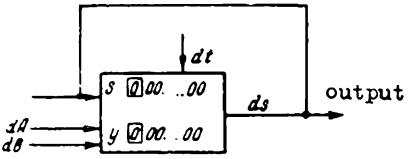

Fig. 18. Comparison of two quantities with the aid of a following integrator.

In the general case, with several channels for the increments dA, dB, dC, etc., the number of overflow pulses at the output of the integrator is the algebraic sum of the increments at all its inputs, i.e.,

$$dS = -(dA + dB + dC + \ldots). \tag{17}$$

This means that if any one of the quantities A, B, C gives a pulse (code 1) at any of the dy inputs, the integrand y has the code $\overline{|0|}\,00\ldots001$, and an overflow with code 0 will appear in the feedback circuit. On the other hand, if any one of the quantities A,B,C offers an increment of code 0 to the integrator input, the integrand y has the value $\overline{|1|}\,111\ldots11$. Then the output of the integrator is 1, and the feedback tends to turn the integrand back into $\overline{|0|}\,00\ldots000$.

A following integrator, like a summing integrator, is often used in the solution of various problems. It is essential, for instance, for the obtaining of increment pulses whose number corresponds to the sum of the increments from several channels at the dx input of the following integrator. Only one pulse at a time can be fed to the dx input, but the number of pulses must be equal to the sum of the individual increments.

In the examples we have mentioned, the feedback circuit links the input and output of only one integrator. For the solution of complicated problems, several integrators

can be plugged in to the feedback circuit of a following integrator.

In this case the following integrator plays the part of an operational and solving integrator, and is a sort of "digital controller" of the required quantity.

Let us examine the solving of the equation

$$\left.\begin{aligned} y &= \arcsin f(x), \\ \text{or} \quad \sin y &= f(x), \end{aligned}\right\} \tag{18}$$

where f(x) is a given function of an independent variable satisfying the condition $-1 \leqslant f(x) \leqslant +1$.

It is required to find y satisfying the equation for all values of x.

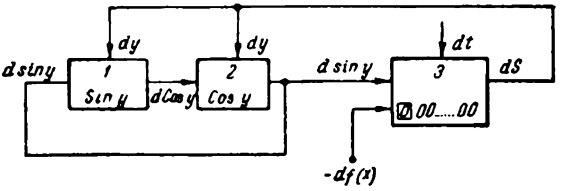

Fig. 19. Solution of y = arcsin f(x).

For the configuration of the circuit shown in Fig. 19 let us suppose y to be known. With the aid of integrators 1 and 2 we form the function sin y. The increment difference $d(\sin y) - df(x) = d\Delta$ is supplied to the dy input of the following integrator 3, and the integrand has initially the code $\overline{0}\,00...00$. We supply the overflow pulses dS of the following integrator as feedback to the inputs of integrators 1 and 2, as the increments dy. Then the following integrator 3 tends to control the dy increments in such a sense that the difference $\sin \alpha - f(x) - \Delta$ decreases to zero. If $\sin y > f(x)$, we have at the output of the following integrator the sequence 0,0,0, etc., which diminishes sin y.

If $\sin y < f(x)$, the sequence 1,1,1, etc. occurs at the output of the integrator, which increases sin y.

Thus y is controlled by means of a following integrator, as in an ordinary servo system.

The speed of working out of the required value for y depends on the scales taken for the overflow pulses supplied to the dy input across the feedback circuit. To increase this speed, overflow pulses can be supplied to the dy input in a scale greater than unity. This is achieved by multiplying them by a coefficient $k>1$ in an intermediate scale integrator (see section 10), or by transferring the dS increments to the second, third or higher digit place of the counter of the y register. This is equivalent to multiplication of dS by a coefficient which is a multiple of two.

In the general case, a chain of several integrators can be plugged into a feedback circuit, and the choice of the necessary scales is made by calculating them when drawing up the programme.

Following integrators are widely used for the formation of diverse functions in the solution of a problem. They make possible the use of the most economical schemes, with small numbers of integrators. We will give some examples.

(1) Forming the function $\sqrt{u}$. The equation for the function $u=(\sqrt{u})^2$ can be written in the form:

$$2\sqrt{u}\,d\sqrt{u}-du=0. \tag{19}$$

The scheme for the solution of this equation (Fig. 20), requires two integrators, of which 2 is a following integrator. It compares the two sides of the equation, and

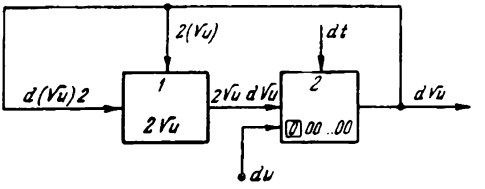

Fig. 20. Forming the function $\sqrt{u}$.

controls the function $\sqrt{u}$ in such a sense that it satisfies the equation.

(2) Forming the product of three factors u,v,w. The circuit shown in Fig. 21a produces the solution of the equation

$$d(u, v, w) = (uv)\,dw + wd(uv), \tag{20}$$

where $duv = vdu + udv$.

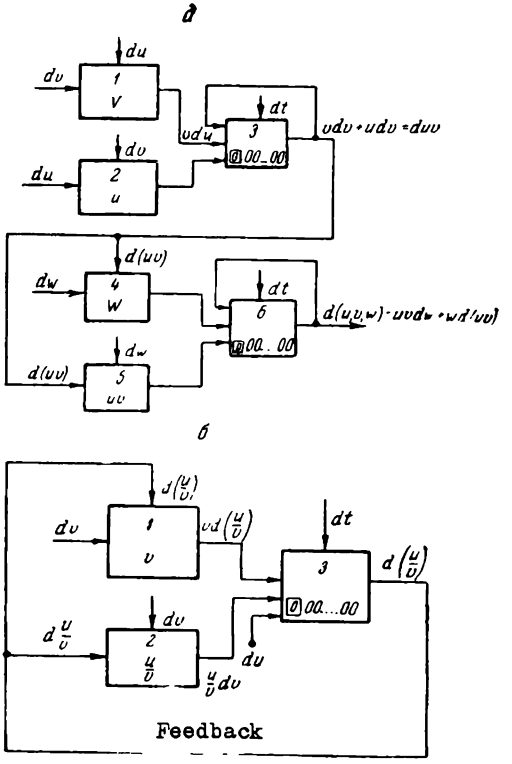

Fig. 21. a) formation of the product u.v.w. b) formation of a quotient.

The following integrators 3 and 6 perform the summation of the two terms fed to the dy inputs of these integrators. The output of integrator 6 is the increment d(u,v,w) in the form of pulses which, accumulating in the counter, give the required product u.v.w. for the given initial conditions.

(3) Forming the function $w = \frac{u}{v}$ (an operation of division). In differential form, this equation can be written as

$$v\,dw + w\,dv - du = 0, \tag{21}$$

or, substituting the value $w = \frac{u}{v}$, we get:

$$v\,d\left(\frac{u}{v}\right) + \frac{u}{v}\,dv - du = 0. \tag{22}$$

This equation is solved by the aid of three integrators (Fig. 21b). Other more complicated functional dependences can be presented by similar methods.

10. Scale Coefficients

The limited capacity of the y and S registers of an integrating machine leads to the necessity of establishing a scale for all the quantities with which the machine is to operate. To each quantity in the machine there corresponds a certain scale $M = 2^m$, where 2 is the radix of the binary system, and m is the power to which we must raise 2 to obtain M.

The scale M shows what one unit of a quantity introduced into the machine corresponds to.

For instance, if a certain quantity A is introduced into the y register of the machine with a scale $M = 2^3$, this means that one unit of the quantity A is represented in the machine by eight pulses.

Let us in future call the power m (for scale M) the scale coefficient. As a rule, all quantities are presented in an integrating machine as numbers in the binary or decimal systems. For this reason the scale coefficient m can only be an integer, which indicates that one unit of a given quantity is presented in the machine in the form of a number 2^m of pulses, and that to store one unit of the given quantity in the y register requires a capacity of 2^m.

First of all, let us establish the correlation of the scale coefficients for one integrator.

Let us denote by m_x, m_y, m_s the scale coefficients for

the input quantities x and y and the output quantity S of the integrator. If the y and S registers of the machine have n binary digit places each, then, as was found in section 2,

$$dS = \frac{1}{2^n} y\,dx. \tag{23}$$

If the increments dx, dy, dS are introduced into the machine with scale coefficients m_x, m_y, m_S, we can write the real correlation between the quantities x, y, S in the form

$$2^{m_S} \cdot dS = \frac{1}{2^n} \cdot 2^{m_y} \cdot y \cdot 2^{m_x} dx, \tag{24}$$

whence it follows that, taking the scales of the input quantities into consideration, the value of the increment dS is

$$dS = 2^{m_y + m_x - m_S - n} \cdot y\,dx. \tag{25}$$

It is desirable to have the increment dS in the same scale as y.dx, that is, we must have dS = y dx. To this end, in (25) the coefficient for y dx must be unity, i.e.,

$$m_x + m_y - m_S - n = 0. \tag{26}$$

Equation (26) is the basic correlation for the scale coefficients of one integrator. It establishes the dependence between the number of digit places n in the registers of the machine, the scale coefficients of the input quantities y and x, and the scale coefficient for the value of the integral at the output of the integrator.

The capacity of the y register, i.e., the number n of digit places that it must contain, is determined by two quantities; the first is the scale coefficient m_y for the integrand, and the second is the maximum value of the integrand y, which, with the given scale, can attain a value of $2^{m_{y\max}}$, where $m_{y\max}$ is the maximum value of the power of 2 corresponding to

$$y_{\max} = 2^{m_{y\max}} \cdot 2^{m_y}. \tag{27}$$

The number of digit places n of the y register must obviously be greater than (or equal to) the sum $m_{y\max} + m_y$, i.e.,

$$\boxed{n \geqslant m_{y\max} + m_y}. \tag{28}$$

The value $m_{y\max} + m_y$ represents the number of digit places in the y register necessary for storage of the maximum value of y.

If at the time of selection of the scales $m_{y\max}$ is unknown, since the maximum of the integrand is unknown the capacity of the y register may be inadequate for the selected scale coefficient m_y. In this case the integrating machine, on reaching the limit of the capacity of the register, automatically stops, the solution is interrupted, and the scale coefficient m_y has to be chosen afresh.

From (26) and (28) we get the following dependence:

$$\boxed{m_x - m_S \geqslant m_{y\max}}. \qquad (29)$$

In fact, $m_y = m_S - m_x + n \leqslant n - m_{y\max}$, or $m_S - m_x \leqslant -m_{y\max}$.

In choosing scales for mutually interconnected integrators (in accordance with the programme), we can pass consecutively from one integrator to another, making use of the following method of calculating scales.

Let $(m_S)_1$ be the scale coefficient for the dS output of the first integrator. We find the scale $(m_S)_1$ from equation (26), expressing it in terms of the scale coefficients m_x and m_y. In the same way we fix the scales for the second, third, etc., integrators.

If several increments from the outputs of other integrators are supplied to the dy input of any one integrator, the scale coefficients for these outputs must have identical values. This secures agreement of all scale coefficients.

For each of the integrators, in accordance with (29), we can write a series of inequalities, which must jointly satisfy

$$\left.\begin{aligned} m_{x_1} - m_{S_1} &\geqslant m_{y_1\max}, \\ m_{x_2} - m_{S_2} &\geqslant m_{y_2\max}, \\ &\cdots\cdots\cdots \\ m_{x_k} - m_{S_k} &\geqslant m_{y_k\max}. \end{aligned}\right\} \qquad (30$$

The joint solution of these inequalities determines the required scale coefficients m_x, m_y, and m_S for each integrator.

Using equation (24), we can establish from the given number of digit places n in the y and S registers the scale coefficients of all remaining variables, or, on the other hand, we can establish from the values chosen for m_x, m_y, m_S the required number of digit places for the registers.

In both cases it is necessary to bear in mind that an increase of the independent variable by one binary digit doubles the time of calculation (i.e. the number of steps). Thus doubling the accuracy of the calculation is achieved at the cost of increased time, and decrease of the time of calculation at the cost of diminished accuracy. This means that increase of speed of calculation can be realized in the form of either increased accuracy of calculation or of diminished time of calculation. In fixing the scale coefficients, the need often arises of multiplying the result

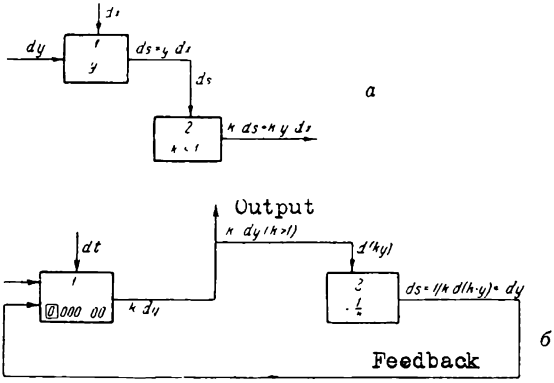

Fig. 22. Scale integrators.

of integration by a certain constant scale coefficient k. This is done by the aid of a so-called scale integrator. If the multiplier $k < 1$, scale integrator 2 is used (Fig. 22a), in which the constant $k < 1$ is introduced as the integrand.

At its output we get

$$k \cdot dS = ky \cdot dx. \tag{31}$$

It is also possible to carry out the multiplication of dy or dS by the constant multiplier $k > 1$. This enables

us to increase, by k times, the number of overflow pulses at the output of the integrator, and in some cases to increase the accuracy of calculation. The circuit shown in Fig. 22b brings about the multiplication k.dy by means of following integrator 1 and integrator 2.

Let us suppose that the number $-\frac{1}{k}$ is introduced as the integrand of integrator 2, and that d(k.y) is fed into the dx input as the independent variable. Then at the output of integrator 2 we get the increment

$$dS = -\frac{1}{k}d(k \cdot y = -dy). \tag{32}$$

The following integrator 1 compares the dy increment of the given function with the increment - dy from integrator 2 in the feedback circuit.

Overflow pulses are generated at the output of the following integrator until the unbalance at its input becomes zero. In this case, the number of overflow pulses at the output will be k times more than at the input, i.e., k.dy, where $k > 1$.

In the solution of certain problems the necessity arises of restricting the value of the integrand between

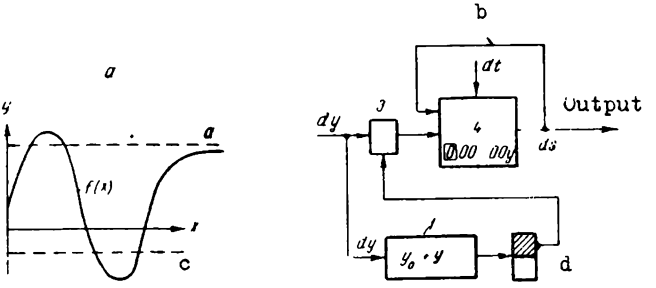

Fig. 23. Restriction of the integrand.

two limits, a and b (Fig. 23a). This restriction can be realized, for instance, with the aid of a circuit containing a restricting integrator 1, a y register which is used for recording a certain number y_0 defining the limit of the restriction (Fig. 23b).

When the value of the function y is such that an over-

flow of the register $y_0 + y$ is produced, the overflow pulse, passing flip-flop 2, closes gate 3 by energizing the inhibitor line, and the increment dy is not applied to the input of the following integrator 4. While gate 3 is closed, the dy increments at the input of the integrator are reproduced at its output. Beyond the limits of the restriction, integrator 4 gives at its output the sequence of overflow pulses 1,0,1,0,1,0... i.e., the increment of the function y becomes zero.

11. Special Cases of the Formation of Functions

A very useful characteristic of the digital integrator is the change of sign of overflows at the output, in accordance with the presence of code 0 or 1 in the last (highest) digit place of the S register (see section 4). This property is utilized in a series of special cases of formation of functions, where the sign of a certain variable-sign function controls the codes of the increments at the output of another integrator.

Let us suppose that one integrator has in its y register a variable-sign integrand f(x). The sign cell (sign code) of this function sets code 1 or 0 in the last (highest) S register of the other integrator. In this case, if the integrated function f(x) of the first integrator is positive, the overflow output dS of the second integrator is unchanged (code 0 in the left-hand digit place of the S register of the second integrator).

If the integrand f(x) of the first integrator is negative, the output dS for the overflow of the second integrator is inverted. That is, if the ordinary output has code 0, there will now be code 1, and vice versa. To this end, in the case of a negative sign for f(x) code 1 appears in the last digit place of the S register.

The scheme shown in Fig. 24 makes use of this property to transform the variable-sign function f(x) into the function $|f'(x)|$, which does not change sign, but has the absolute value of the function f(x). Here something like a full-wave rectification of a sinusoidal function takes place. Integrator 1 serves for the integration of the function $y' = f'(x)$. At its output we get the increment $dy = df(x)$ of the variable-sign function. The increments dy are stored in the y register of integrator 2. The sign code of the y register controls the code of the last S register of integrator 3 in such a fashion that

to a code 1 in the y sign cell there corresponds a code 0 in the last digit of the S register of integrator 3, and vice versa. Thus when the sign of f(x) is positive, the overflow pulse codes dS of integrator 3 do not change.

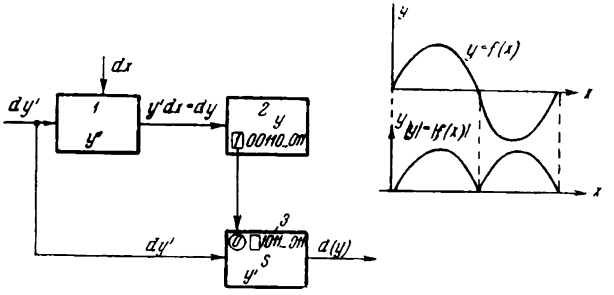

Fig. 24. Transformation of the variable-sign function f(x) into $|f(x)|$.

In consequence, integrator 3, to the input of which the increments dy' are also supplied, forms at its output increments of the function f(x) = dy. If the sign code of f(x) in integrator 2 is 0 (that is, f(x) is negative) the overflow codes at the output of integrator 3 have the opposite sign, and so increments of the function $-|-f(x)|$, that is, $+f(x)$, are produced at the output of integrator 3.

Thus in both cases we get positive valued increments of the function $|f(x)|$ at the output of integrator 3, i.e.:

a) if $f(x) \geqslant 0$, the output of integrator 3 is $+ f(x)$,

b) if $f(x) < 0$, the output of integrator 3 is $-|-f(x)|$.

Let us examine an example of the use of an integrator controlled by a variable-sign function for the solution of the differential equations

$$\left.\begin{aligned} &\frac{d^2y}{dt^2} + k_1 y = 0, \quad \text{if } y \geqslant 0 \\ \text{or} \quad &\frac{d^2y}{dt^2} + k_2 y = 0, \quad \text{if } y < 0. \end{aligned}\right\} \tag{33}$$

Here, depending on the sign of the required function y, we must move from one equation to the other, in which the coefficient k_2 has a new value. Thus, depending on the region of the solution of the problem, we must move from

one equation to the other when, as a result of solution, it happens that the function required crosses the boundary between one region and the other.

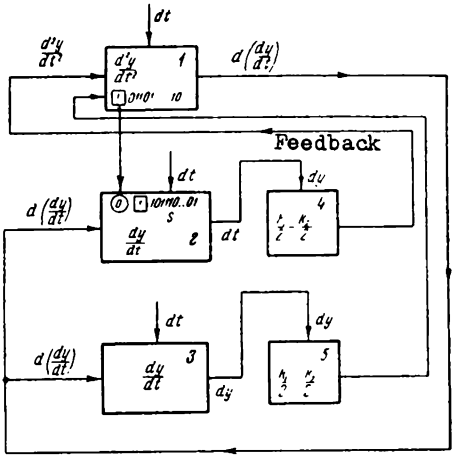

Fig. 25. Solution of differential equations with variable coefficients.

The scheme shown in Fig. 25 produces the required solution of the problem. The code of the last digit of the S register of integrator 2 and the overflow pulse code at its output change in accordance with the sign of the integrand $\frac{d^2y}{dt^2}$ of integrator 1. The equation can be written in the form:

$$\frac{d^2y}{dt^2} = -k_1 y \text{ or } \frac{dy}{dt} = -k_1 \text{ when } y \geqslant 0, \tag{34}$$

$$\frac{d^2t}{dt^2} = -k_2 y \text{ or } \frac{dy}{dt} = -k_2 \text{ when } y < 0. \tag{35}$$

In drawing up the scheme, we suppose $\frac{d^2y}{dt^2}$ to be known. Then, using integrator 1, we find d(dy/dt), and using integrator 2 or 3 we get the increment dy. The scale integrators multiply the increment by constant factors: integrator 4 by $\frac{k_1}{2} - \frac{k_2}{2}$, and integrator 5 by $-\frac{k_1}{2} - \frac{k_2}{2}$.

If $y>0$ (i.e., $\frac{d^2y}{dt^2}$ is negative) the code of the last digit in the S register of integrator 2 will be 1, and the overflow pulses of integrator 2 will have the inverse code, i.e., $-dy(\frac{k_1}{2}-\frac{k_2}{2})$ at the output of integrator 4. As a result of the summation of the increments of integrators 4 and 5, we get an increment at the output of integrator 1 equal to

$$d\left(\frac{d^2y}{dt^2}\right)=-dy\left(\frac{k_1}{2}-\frac{k_2}{2}\right)+dy\left(-\frac{k_1}{2}-\frac{k_2}{2}\right) \tag{36}$$

or $d(\frac{d^2y}{dt^2}) = -k_1dy$. Therefore in this case the problem is solved according to equation (1).

If $y<0$ (i.e., $\frac{d^2y}{dt^2}$ is positive) the code in the last register S of integrator 2 will be 0, and overflow pulses at the output of this integrator will have the ordinary code. In this case the sum of the increments of integrators 4 and 5 will be

$$d\left(\frac{d^2y}{dt^2}\right)=\left(\frac{k_1}{2}-\frac{k_2}{2}\right)dy+\left(-\frac{k_1}{2}-\frac{k_2}{2}\right)dy=-k_2\,dy. \tag{37}$$

The problem is thus solved in accordance with equation (2).

12. Introduction of Functions on Punched Tape

Input parameters given in the form of tabular or experimental functions can be fed directly into the machine on punched or magnetic tape. There are two possible ways of writing functions.

First method of writing functions. Discrete values of the increments $df(x)$ of a given function $f(x)$ are written on tape in the form of holes punched in a paper tape or pulses to be read back from magnetic tape. Each pulse corresponds to one unit of increment of the function on the chosen scale, and the sum of the increments (number of pulses) corresponds to the value of the function $f(x)$. That is,

$$f(x)=\sum df(x)+f(x)_0, \tag{38}$$

where $f(x)_0$ is the initial value of the function.

Instead of writing the increments of the function $f(x)$ itself on the tape, we can write the increments of its derivative $df'(x)$. Then the sum of the accumulated increments, in the form of pulses, corresponds to the derivative of the given function. That is

$$f'(x) = \sum df'(x) + f'(x)_0, \tag{39}$$

where $f'(x)_0$ is the initial value of the derivative.

Fig. 26 shows the scheme for writing the increments of a function on punched tape and feeding it into the integrating machine. Here the punched tape 1 is shifted to

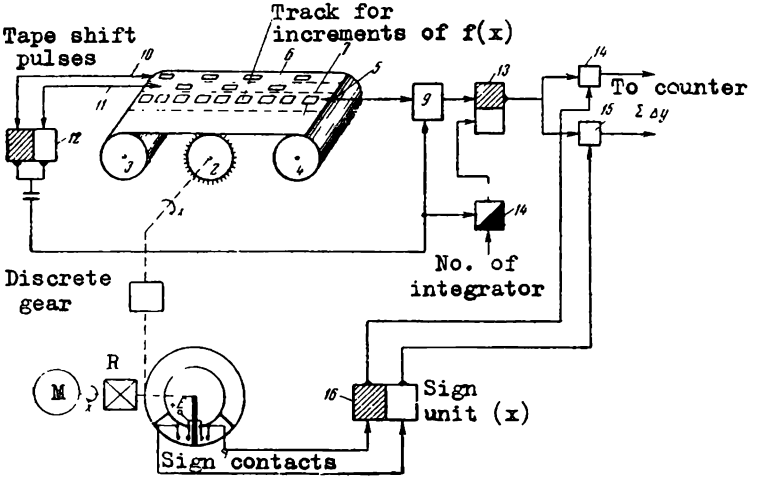

Fig. 26. Writing increments of a function on punched tape.

either side, in proportion to the value of x, by the guiding drum 2, which has fine teeth round the circumference to engage the tape. Tape from drum 3 is wound on to drum 4, or vice versa, depending on the direction of rotation. Increments of functions are written on the tape by punching. The number of holes in a length of tape is proportional to the value of the function, and the density of their distribution is proportional to the derivative of this function. The maximum possible

density of punching corresponds to the maximum value of the derivative of a given function, and as its value decreases, the density of the holes in the tape (number of holes to 1 cm of length) also decreases.

The length of the tape must be such as to secure the required degree of accuracy in the reproduction of the function according to a given law. For instance, if the tape contains 1000 holes in all, corresponding to the variation of the function from zero to the maximum, then one hole corresponds to 0.1% of the maximum value.

As the tape moves, contact head 5 slides over it, counting the holes. When it finds a hole, contact 5 makes contact with a metal plate under the tape, which is connected to the positive terminal of the power supply, and a potential difference appears at the input of gate 9.

The tape has three tracks. In tracks 6 and 7 staggered holes are punched at equal distances along the whole length of the tape; these ensure the movement of the tape by one division at a time. In moving the tape, they act as a kind of clock pulse, being indications of the movement of the tape by one division. At each movement of the tape, pulses read by heads 10 and 11 are supplied alternately to each of the two inputs of flip-flop 12, triggering it. At each triggering of the flip-flop a voltage pulse is supplied from its output to gate 9. If a voltage pulse from the flip-flop coincides with a voltage read by head 5, it is passed by gate 9 to flip-flop 13. This happens if there is a hole (code 1) in the track on which the increments of the function are written.

The code is read from the output of flip-flop 13 at the proper time in pulse form, and is fed into the machine. This is done by sending a clearance pulse to the second input of flip-flop 13 through gate 14. It is sent at the moment when the proper sector of the magnetic drum passes, that is, the sector to which the pulse written on the tape is to be sent. Gate 14 is normally open; it closes only when an inhibiting pulse from flip-flop 12 is sent to its second input at the same time as a movement of the tape. This prevents random loss of pulses written on the tape when a pulse from trigger 12 coincides with an integrator No. pulse, clearing flip-flop 13. The tape is moved by the motor M through the reducing gear R, in proportion to the value of the independent variable x. Movement can be either continuous or discrete. Discrete

movement can be brought about by the use of a Maltese cross, or any other discrete gear. On the shaft, after the reducer, there is mounted a contact unit which determines the sign of the direction of rotation of the shaft. It consists of a lever by which the contact assembly is moved round the circumference of the disc. Depending on the direction of rotation of the shaft, the sign contacts, which control the position of the sign trigger unit 16, complete the circuit. The trigger unit in its turn opens gate 14 or 15, and allows the pulse from the tape to be sent to the addition or subtraction input of the $\Sigma \Delta y$ counter of the integrator. In this way the sign of the increment of the independent variable x is taken into account. All increments of the function f(x) are taken as having the same sign. If f(x) is not a monotonic function, we can easily produce it by writing the sign of the increment df(x) on a special track. If the increment df(x) written on the tape are not only introduced into the integrand of the integrators but are also used for the dx input of an integrator, an intermediate following integrator is used; overflow pulses corresponding to the increment df(x), written on the tape, are obtained at its output.

If df(x) has the code 1 or 0, then 1 or 0 is obtained at the output of the integrator. If the increment df(x) is zero, the output of the integrator is the overflow pulse sequence 1,0,1,0,1,0, etc., as long as the increment remains zero.

To shorten the tape and make it possible for it to move more slowly, we can write on it not the increments of the function itself, but the increments of its derivative df'(x); that is, the second differences. In this case the increments of the derivative accumulate at the integrand input of the integrator, and their sum forms the derivative f'(x). Integrating with respect to x, we get the required function f(x) at the integrator output, since $\int f'(x)dx = f(x)$. At the integrator output we obtain overflow pulses $df(x) = f'(x)dx$, which can be used in the further solution of the problem.

Second method of writing functions. The second method of writing the functions consists of writing on the tape not individual pulses, but codes of the numbers corresponding to the value of the derivative of the function or to the value of its increments.

It is well known that every curve f(x) can be approx-

imated to the required degree of accuracy by a series of straight sections, with the independent variable divided into equal intervals. In each section of the linear approximation the derivative, obviously, keeps its value unchanged, since the tangent of the angle of inclination of the section of a straight line which approximates to the curve f(x) remains unchanged. If we write on the tape 10 to 20 values of the derivatives of the function for 10 to 15 sections of approximation (or, still better, of their increments) this is enough for us to obtain, by the integration $\int f'(x)dx = f(x)$, all the values of the function f(x), with a degree of accuracy of the order of 0.1%.

The codes of the number (increments of the derivative) are written on the tape by punching a series of holes across the width of the tape (Fig. 27). The number

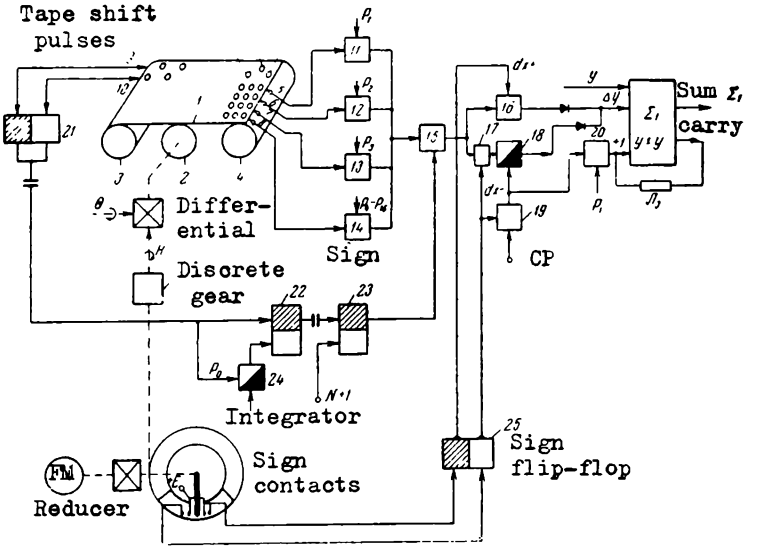

Fig. 27. Writing the increments of a derivative.

of parallel tracks is the same as the number of binary digits in the code of the number, including the sign code. Special tracks with reading heads 9 and 10 are assigned for securing movement of the tape by one division (one number). The code written on the tape is read in parallel

by reading heads 5 to 8. The parallel code of a numbe written on the tape is turned into a serial pulse code by gates 11 to 14. These gates give the code of a number serially as the serial clock pulses p_1, p_2, ..., corresponding to the first, second, third, etc., digits of the code of the number, are supplied to their inputs.

These clock pulses are supplied from the busbars of the rectifier network of the pulse counter in the integrating machine. If the number of digits of the written code is less than the full number of digit places in the y register, the codes of all the higher digit places are the same as that of the sign of the number. This secures correct summation of the code of the derivative of the function written on the tape, and the code of the derivative held in the y register of the integrator.

According to the direction of movement of the tape, the code of the increment $df'(x)$ is added to or subtracted from $f'(x)$ in the y register. If the increment of the argument dx is positive, the direct code of the number on the tape is supplied to the adder Σ_1 through gate 16. If the increment dx is negative, the inverse code of the number is supplied to adder Σ_1 through gates 17 and 18. The inverse code of the number is formed by the coincidence circuit 18, which transmits a clock pulse to the input of the adder when the code recorded is 0, but not when the code is 1. In other words, it inverts the code. For correct calculation we have to add the complementary code of the number on the tape; that is, the inverse code plus one unit in the lowest digit place. The addition +1 is made by gate 20, which transmits to the adder a clock pulse for the first digit place p_1.

Codes written on the tape are read out at the proper time by gate 15, once for each movement of the tape by one division. Flip-flop 21, which controls the movement of the tape, works in the same way as flip-flop 12 in the previous scheme. At each operation of flip-flop 21, flip-flop 22 is triggered. This flip-flop is cleared by a pulse at the beginning of the sector (integrator No.) to which the code on the tape is to be transferred. When this happens, flip-flop 23 is activated, holding gate 15 open during the addition of the codes in the machine. Gate 15 closes at the beginning of the next sector, when flip-flop 23 is cleared. Flip-flop 25 determines the

sign of the increments of the argument x, and controls gates 16, 17, and 19, as in the previous scheme. The advantage of writing the increments of the derivative on the tape rather than the derivative itself lies in the smaller number of digits in the code of the number, and the smaller number of reading heads.

With this small number of codes we can use a punched cylinder of insulating material. Holes are punched on the surface of the cylinder, in accordance with the code of the derivative. A metal cylinder is inserted in the insulating cylinder and connected to one of the poles of the source of potential. With discrete rotation of the cylinder one code or another for the derivative f'(x) is presented to the contact heads.

A cylinder of 44 mm diameter and 50 mm length can accommodate about 40 binary codes of numbers each having 14 binary digits. This number of codes for a derivative is quite sufficient to produce a function (a sine, for instance) with an error of the order of a hundredth of one per cent.

We have supposed that the tape or cylinder has written on it derivatives or increments of a derivative corresponding to a linear approximation of the curve $y = f(x)$. Other methods of approximation of the curve are, however, possible. For instance, with quadratic approximation each section of the curve approximates to a section of a parabola whose equation can be written in the form:

$$y = ax^2 + bx + c, \tag{40}$$

where a, b, and c are constant coefficients for the given section of the approximation.

Differentiating y by x twice, we get:

$$\frac{dy}{dx} = 2ax + b; \quad \frac{d^2y}{dx^2} = 2a. \tag{41}$$

Hence it is clear that the second derivative for a given section is constant and equal to 2a. As for the first derivative, it is linearly dependent on x.

We can form the function given in (40) by means of two integrators (Fig. 28). To do this, it is enough to give the value of the integrand in the first integrator as 2a, and to set the initial value of the integrand as equal to b, and the initial value of the integral equal to c in the second integrator. Then, integrating by the

independent variable x, we obtain the function y in accordance with equation (40).

Quadratic approximation permits us to decrease the number of sections of the approximation to three or less

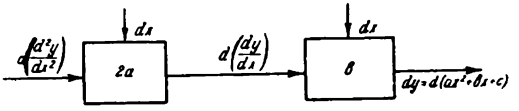

Fig. 28. Scheme for quadratic interpolation.

for the whole range of variation of x. The number of sections depends on the degree of accuracy required, and on the form of the given function y.

To introduce a given function on punched or magnetic tape into the scheme shown in Fig. 28, it is often sufficient to write the values of the coefficient a (or of the increment Δa) for each section of the approximation. In this way we can determine a number of points of the curve $y = f(x)$, and can then obtain by interpolation a point for any value of x. This process of interpolation reduces to an integration operation. For linear interpolation one integrator is required; for quadratic interpolation we need two, and for cubic interpolation three. The integrators of the digital integrating machine are used for this.

The advantage of quadratic and cubic interpolation is the high degree of accuracy attained in producing a function with a very small number of sections of approximation.

13. Introduction of Functions in the form of Graphs

A function given in the form of a graph can be introduced directly into an integrating machine by means of an external function unit. The function unit (Fig. 29) consists of a drum (1) with the graph of the function, drawn in conductive ink on paper, wrapped round it. The shaft (x) of the drum is turned through an angle proportional to the argument x. The potentiometric tracing head 2 moves the following motor FMy, by aid of the worm gear 4, so that it follows the curve $y = f(x)$.*

*A graph-reading unit is described in Ref. 22.

With deviation of the centre of the tracing head from the curve, a voltage Δu, proportional to the magnitude of the deviation, appears.

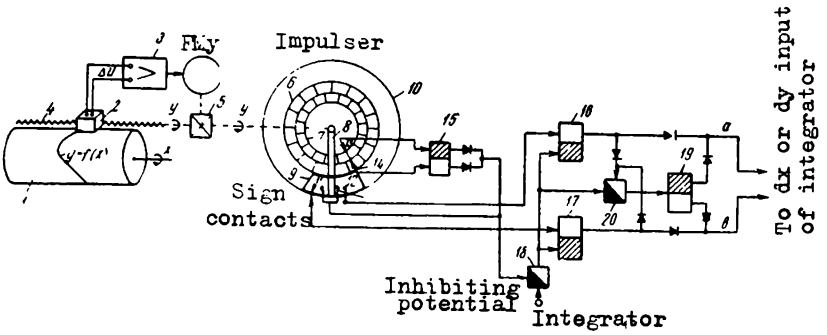

Fig. 29. Introduction of functions in the form of graphs.

The error voltage Δu is amplified by the amplifier 3, which controls the following motor FMy. Continuous tracing of the curve is obtained by means of the following motor.

The impulser, which transforms the angular displacement of the shaft into a proportionate number of pulses, is connected to the shaft of the following motor FMy through the reducing gear 5. This is achieved by the two contact discs 6 and 7, the contacts of which are displaced with regard to one another by one contact division.

The blade 8, which shifts the contact assembly 9, is rigidly connected to shaft y. The assembly 9 is pressed against the disc 10 by a spring, and moves around the edge of it in guiding grooves. As the assembly moves, the blade 8 closes the left or right contacts 11 or 12, which determine the direction of rotation of the shaft. Between contacts 11 and 12 there is a small gap, the size of which is determined by the admissible zone of insensitivity for the angular displacement of the shaft. The brushes 13 and 14 are mechanically connected with the assembly 9; they slide over the two contact discs 6 and 7, which have insulated contact plates.

All the contact plates are connected to one pole of the source of potential. On movement of the brushes 13 and 14, voltage pulses are received alternately at each input of flip-flop 15, as the brushes make contact with the

plates. Each pulse triggers the flip-flop, which produces square pulses (positive or negative) which are transmitted by flip-flops 16 and 17, depending on the direction of rotation of the shaft y. When flip-flops 16 and 17 are restored to their initial cleared position, a pulse code corresponding to the increment of the shaft y (+1 or -1) is sent to the dy or dx input of the appropriate integrator. Flip-flops 16 and 17 are cleared by means of the gate 18 (a coincidence circuit) which transmits a pulse from the busbar of the appropriate integrator at the correct moment.

To obtain the pulse code sequence 1,0,1,0,1,0, etc., at the input of the integrator when there is no increment pulse from the y shaft, we use the supplementary flip-flop 19 and the coincidence circuit 20. If there are no increment pulses from the y shaft, flip-flop 19 is triggered at every step of the integration, and sends pulses alternately to buses a and b, corresponding to 1,0,1,0, 1,0 etc. at the integrator input. If there is an increment pulse from the y shaft, coincidence circuit 20 does not pass a pulse to flip-flop 19.

In this way the increments of the y shaft, transformed into pulses, are fed to the appropriate integrator.

Any function $y = f(x)$ presented as a graph can be written in code form on punched tape by means of a comparatively simple mechanism. This tape can be used to feed the given function into the machine. One graph unit will serve to feed many functions into the machine.

Fig. 30 shows the mechanism for converting a graph into code form on punched tape. The graph unit, consisting of the drum 1, potentiometric tracing head 2, amplifier 3, and following motor FMy on the y shaft are as described above.

The punched tape 6 is moved on the shaft of the independent variable x simultaneously with the drum 1. Discrete movement of the tape, once for every step (one division) is secured by the discrete gear 7. This can be the gear used in electromechanical counters, or a Maltese cross etc. An angular increment of the x shaft, of determined magnitude, moves the tape each time by one division between the holes punched in it. The punching of holes in the tape corresponds to the independent variable x, and is done as follows. At each displacement of the x shaft by a magnitude corresponding to one division Δx, the

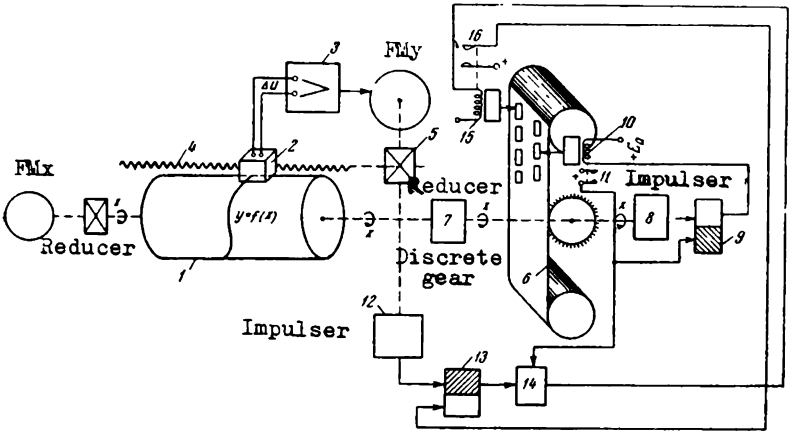

Fig. 30. Writing a graphically presented function on punched tape.

electromechanical impulser 8 delivers a pulse which is transmitted by flip-flop 9. This energizes the electromagnet 10 of the perforator, and the perforator punches a hole in the x track of the tape. As the hole is punched, the contacts 11 of the perforator electromagnet make contact, and a voltage pulse clears flip-flop 9, so that the electromagnet returns to its initial state.

If during a displacement of the x shaft by the magnitude Δx an increment of y takes place, the impulser on the y shaft delivers a pulse which is transmitted by flip-flop 13. This flip-flop controls gate 14, which (when there is a Δy increment) delivers a voltage pulse from the contacts 11 to the electromagnet 15 of the y track perforator. A hole is thus punched in the y track after the punching of a hole in the x track, and the holes in the x and y tracks are punched in one line. After the hole is punched in the y track, 13 is restored to its initial state by a pulse as the contacts 16 of the perforator electromagnet make contact.

Movement of the tape by the motor FMx, and tracing of the curve $y = f(x)$, must be slow enough to allow time for punching holes. The feeding of functions from the punched tape into the machine can be considerably speeded up if the second differences (increments of the derivative of the function) are written on the tape.

14. Graphical Presentation of the Results of Calculation

The results of calculation can be presented in the form of a graph, by using a graphic function unit (Fig. 31).

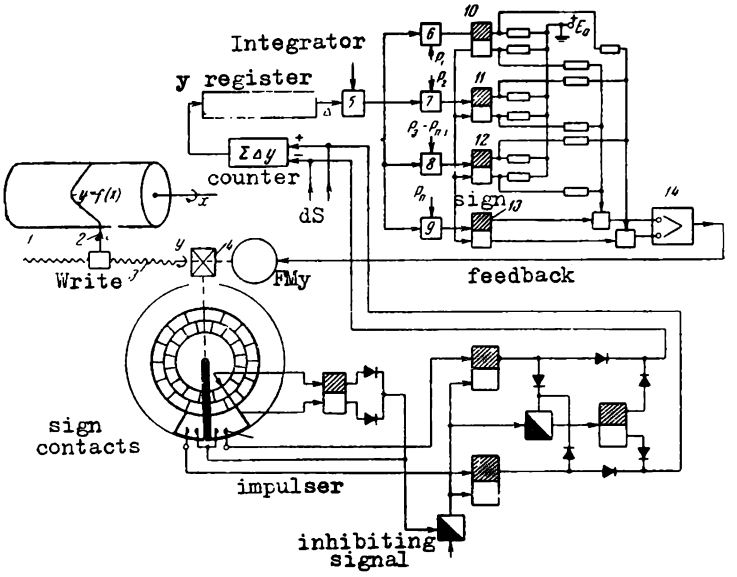

Fig. 31. Graphical presentation of the results of calculation.

The result is held in the y register of the integrator. Accumulation of dy increments in the y register of this integrator proceeds step by step with the integration. The dy increments for the calculated value of y are supplied from the dS line to the $\Sigma \Delta y$ counter, and thence to the y register. Increment pulses dy are fed back to this same counter and register from the graph recording unit. In view of this, the y register of the given integrator holds a number equal to the difference $\Delta = y_{cal} - y_{dev}$, where y_{cal} is the calculated value, and y_{dev} is the magnitude developed on the y shaft of the graphic function unit.

The difference Δ, in the form of a potential, controls the following motor FMy, which presents the calculated

value of y in the form of a mechanical displacement of the y shaft of the graphic function unit. The unit consists of the drum 1, on the surface of which the graph of the function $y = f(x)$, calculated by the machine, is automatically traced by the writing head 2. The writing head is moved along the drum by the worm gear 3. It is set in motion by the following motor FMy, through the reduction gear 4.

The movement of writing head 2 is transformed into pulses by an electromechanical impulser, as in the system shown in Fig. 29. Pulses corresponding to the determined increment Δy are supplied as negative feedback to the input of the $\Sigma \Delta y$ counter of the given integrator, to which increments of the calculated quantity y_{cal} are also supplied. In consequence, the y register holds the value of the difference Δ between the calculated and developed values of y. The code for Δ received from the writing head of the y register is presented in the form of a series of pulses to the converter unit through gate 5, which opens for the address of the given integrator. This code is transferred serially by the flip-flop units 10 to 12, and the code for the sign of Δ is transferred by circuit 13. Pulses are transmitted to the flip-flop circuits through gates 6 to 9, which are opened in succession by pulses p_1, p_2, ..., p_n from the diode matrix of the digit counter. Gate 8 is opened by any pulse from the third to the $p - 1^{th}$. The last pulse p_n opens gate 9, admitting the sign code for Δ.

It is not obligatory to have as many flip-flop circuits as there are digits in the code of the number Δ in order to control the motor. It is sufficient, for instance, to transfer the lowest two or three digits of the code of Δ by aid of flip-flops 10 and 11.

In fact, the difference $\Delta = y_{cal} - y_{dev}$ in the control process must be small, and 2 or 3 digits of Δ are enough for smooth control of the speed of the motor FMy. If this difference is greater, i.e., if code 1 appears in any of the higher digit places, it is transmitted by flip-flop 12. This secures maximum speed of the motor FMy.

The state of flip-flop circuits 6 to 8, holding the code of the number Δ, is converted into an electrical potential controlling the motor FMy. A sum of potentials

proportional to the code of Δ is obtained at the output of the summing amplifier 14. This amplifier controls the following motor Mxy, to which the feedback of the control circuit is connected. As a result the curve $y = f(x)$ inscribed on the drum accurately reproduces the calculated values of y, since every increment dy of the calculated value for y is developed by the following motor Mxy in the form of a corresponding mechanical movement, thanks to the feedback loop.

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P. P. GOLOVISTIKOV

DYNAMIC FLIP-FLOPS AND THEIR USE IN PARALLEL ACTION COMPUTERS

1. Dynamic Flip-flops with Delay Lines. The Use of Dynamic Flip-flops in Shift Circuits

"Dynamic flip-flop" is the accepted term for a circuit holding code 1 in dynamic form, as a pulse continuously circulating in a delay-line circuit.

Clock pulses are supplied continuously to the dynamic flip-flop at a constant rate. If they find the circuit in code 0 position they do not affect it; but if it holds code 1 they continuously compensate the loss of the pulse circulating in the delay line. The dynamic flip-flop, if it is in position 1, continuously puts out pulses synchronous with the clock pulses. If it is in position 0, no pulses appear at its output. One or other of these processes is set going by start pulses supplied to one of the two inputs, S1 and S0. A pulse from S1 can only set the flip-flop in position 1, and a pulse from S0 can only set it in position 0. Many variants of the dynamic flip-flop are possible, differing in the method of triggering.

Fig. 1 shows the two most efficient variants of dynamic flip-flop circuits. We have investigated these and other circuits.

Let us consider the working of the circuits in Fig. 1. We will suppose that both circuits are in position 0. This means that no pulse is circulating in the circuits, and the clock pulses (Cl) are not passing the coincidence gate (Gc), since there is no signal at the other input of the gate. If an S1 pulse is applied at the same time as

the clock pulse, the coincidence gate Gc puts out a signal. In circuit (a) this signal passes through the anti-coincidence gate (Ga). An output signal is applied from the delay-

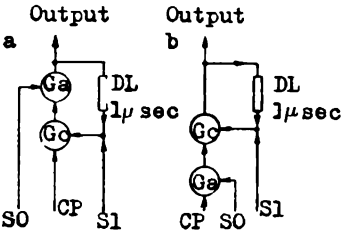

Fig. 1. Two variants of the dynamic flip-flop.

line (DL) to the input of the gate Gc simultaneously with the next clock pulse CP. Thus a second signal passes the output, and this provokes a third, etc. The circuit continues to put out pulses until an SO pulse is supplied simultaneously with a clock pulse. This pulse inhibits the signal sent to the output by gate Gc through the anti-coincidence gate Ga in circuit (a), and prevents the clock pulse reaching the coincidence gate Gc in circuit (b), where, in consequence, there will be no signal at the output. The next clock pulse will not reach the output of either circuit, since there is no signal at the other input of the coincidence gate Gc.

Thus the dynamic flip-flops remain in position 0 until the next S1 pulses are supplied.

The following conditions must be observed for proper functioning of both schemes.

1) Correct phasing of the SO, S1, and clock pulses must be secured. These pulses must be synchronous.

2) All elements of the recirculation circuit must have a delay time equal to the interval between two successive clock pulses.

3) In order that small variations of the parameters of the circuit or of its operations should not upset the proper functioning of a dynamic flip-flop, the pulse supplied by the delay line to the input of the coincidence gate Gc must be somewhat wider than the clock pulse. If

for any reason there is a change in the rate of the clock pulses, or of the delay in the recirculation circuit between clock pulses and narrow pulses from the delay line, there will be a time discrepancy. There is then either no signal at the output, or it is narrower than either pulse separately. In the latter case the third pulse will be still narrower and smaller, and eventually the signal will be lost.

If the delay line supplies a signal wide enough to include the duration of the clock pulse, the circuit puts out a normal pulse which, widening as it passes through the delay line, overlaps the next clock pulse. The wider the pulse at the input of gate Gc, the greater the range of rates of succession of clock pulses with which the circuit can work. Experience of the working of dynamic flip-flops has shown that half as much again is the most efficient widening of the signal from the delay line.

A very wide signal can go to the other extreme. With a small variation in the parameters of the circuit or the rate of succession of clock pulses, the next clock pulse may coincide with the wide pulse. The output of such a circuit will be random. It is easy to show, on the other hand, that with wide clock pulses and narrow pulses in the delay line the system will not work.

4) The recirculation circuit of a dynamic flip-flop must include a shaping and amplifying element. This element must regenerate accurately a distorted pulse applied to its input from the recirculation circuit. The reliability of working of the system depends on the regeneration of the signal by the shaping element. The system will work reliably only if the shaping element regenerates even a small signal to normal pulse size. An amplifier is essential. Ga in Fig. 1a or Gc in Fig. 1b can be the shaping element, or there can be an additional element in the recirculation circuit.

The dynamic flip-flop has a number of significant advantages over the ordinary trigger circuit.

1) The circuit of the dynamic flip-flop is a good deal simpler than that of the trigger circuit. It includes many fewer resistors, capacitors, and other components. The circuit of the dynamic flip-flop is easy to build. It uses one miniature valve while the ordinary trigger circuit uses two valves.

2) The dynamic flip-flop puts out pulses, not potentials;

this considerably simplifies its connexion to pulse-operated germanium diode gates.

3) The output circuit of a dynamic flip-flop can take the form of a shaping valve which has a transformer with a high transfer ratio in its anode circuit. A flip-flop of this kind can produce pulses of considerable power, whereas the trigger circuit, as is well known, can work only with small loads.

4) The dynamic flip-flop has a very high speed. The first pulse at the output of the circuit (synchronous with an S1 pulse) can be used to control other circuits. The trigger circuit can control other circuits only when the transient processes are completed.

5) A dynamic flip-flop can be more reliable than a trigger circuit. This is obvious from the fact that a dynamic flip-flop is a crude amplifier. For correct working, the output signal should be not less than a specified value. Questions of reversal and of symmetry, which are of fundamental importance for the trigger circuit, have no meaning here.

However, the dynamic flip-flop has also a number of defects, which can limit its application in a number of systems.

1) The dynamic flip-flop requires accurate phasing of input signals.

2) Since it requires accurate phasing of input signals, and also delays the output signal (although very briefly), it is not easy to use the dynamic flip-flop in systems which excite each other in series. For instance, for proper operation of a counter constructed of dynamic flip-flops, clock pulses must be shifted for successive digits. This greatly increases the number of components, creates obvious difficulties in operation, and decreases the reliability of the system. For this reason it is inexpedient to use the dynamic flip-flop in counters, or in adders with parallel action, etc. Dynamic flip-flops with delay lines can conveniently be used when co-ordination of input pulses can be easily secured; for instance, in registers for storage and shift of codes.

3) If a dynamic flip-flop is in state 1 and is not actuated by an input signal S0 or S1, it works continuously. Therefore, in units in which code 1 is registered, dynamic flip-flops complete a large number of duty cycles.

4) One absent clock pulse will clear the code which is held in a dynamic flip-flop. Therefore any disturbance which enters the impulser and attenuates a clock pulse to a significant extent can ruin the entire operation of an electronic calculator using dynamic flip-flops.

Let us return to Figs. 1a and 1b. The circuit in Fig. 1b is convenient when an SO pulse has to be supplied simultaneously to a large number of dynamic flip-flops. In this case one Ga gate will serve for all the flip-flops. This greatly simplifies the circuit of each dynamic flip-flop. In shift registers it is also necessary to clear the codes from all flip-flops simultaneously; therefore it is unquestionably better to use the circuit shown in Fig. 1b in registers. When it is not necessary to clear codes simultaneously from all flip-flops, it is better to use the circuit of Fig. 1a, which is more suitable for general purposes.

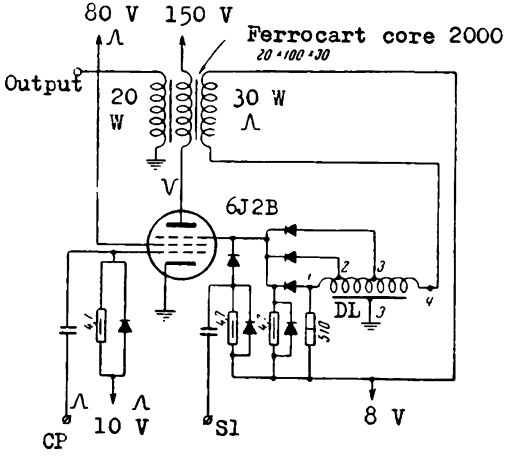

Fig. 2. Dynamic flip-flop with delay line.

Fig. 2 shows the layout of a practical circuit based on Fig. 1b. It has proved satisfactory when used in the register of a specialized counter.

In this circuit a pentode is used for the Gc gate. Wide

pulses from the delay line are applied to the suppressor grid. Narrow clock pulses (CP) are supplied to the control grid. Diodes in parallel with the leak resistance serve for restoration of the d.c. component. A resistance of 510 Ω co-ordinates the delay line with the valve input circuits.

An effective method of widening the pulse from the delay line is used. A pulse corresponding closely in shape and length to the pass-band of the line circulates in the delay line. This pulse is applied to the suppressor grid from taps on the delay line. In this way the grid is actuated by a complex of pulses supplied at different times. Superimposed on each other, they form a wide signal.

The nominal ratings of the circuit are:

anode voltage	150 V
screen grid voltage	80 V
bias on first grid	10 V
bias on third grid	8 V
clock pulses peaky, positive, with basic length 0.3 to 0.4 μsec and amplitude	28 V
S1 pulses peaky, positive, length 0.3 to 0.4 μsec, amplitude	28 V
no S0 pulses; clearance is by elimination of a clock pulse; mean operating range (frequency of clock pulses)	720 to 1000 kc/s

In a dynamic flip-flop circuit the resistors and capacitors can have a 10% tolerance, and the valve can have a characteristic spread of ± 20%. Diodes can be used which have a spread of about 200% in direct resistance and about 400% in back resistance. The magnitude of delay and the impedance of the delay line can vary within 10%. A standard delay line type III, as produced by the radio-engineering industry, is used.

Fig. 3 shows the output-pulse transformer, with a diode for comparison. Fig. 4 shows oscillograms of voltages in different parts of the circuit, and Fig. 5 shows the averaged basic characteristics of the flip-flop.

From an examination of the characteristics of this type of dynamic flip-flop we can draw this conclusion: with

variations of conditions within quite wide limits, the range of operational frequencies, (and therefore the reliability of working) remain approximately unchanged.

Fig. 3. Pulse transformer of the dynamic flip-flop shown in Fig. 2.

When these limits are reached, the range of frequency contracts to zero; and when the limits are passed, the flip-flop stops working. Thus we can secure reliability by operating well within the limits.

Fig. 6a shows the block scheme for a register for storage and shift of codes, constructed with flip-flops of the kind described above.

The anti-coincidence gate has been removed from the basic register circuit to the control circuit, as it is necessary to set all digit places at "0" simultaneously when a shift takes place. In each digit place, in parallel with the coincidence gate of the flip-flop, there is yet another coincidence gate, to whose input a shift pulse is supplied from the anti-coincidence gate. The shift pulse always coincides with the generation of a clock pulse. However, no clock pulse is applied at this time, since an SO pulse inhibits it at the anti-coincidence gate. A widened pulse from the delay line of the preceding digit is applied to the second input of the coincidence gate in the shift circuit.

Since the shift pulse is equivalent to a clock pulse, the gates work in identical conditions; when the coincidence gate of the flip-flop does not operate, the gate of the shift circuit transfers to the flip-flop the code

Fig. 4. a) clock pulses b) S1 pulse c) pulses at grid three d) pulses in delay line e) pulses in an output load equal to 1.0 kΩ. (the vertical and horizontal lines indicate 20 V and 1 μ sec respectively).

which is held in the preceding digit place.

Shift in the register is carried out as follows. As in normal practice, the code of the number is supplied to all digit places of the register simultaneously. This code can be stored in the register for any length of time, as a result of the action of the clock pulses, which normally pass through the anti-coincidence gate. In order to bring about shifts, S0 pulses are applied. Each S0

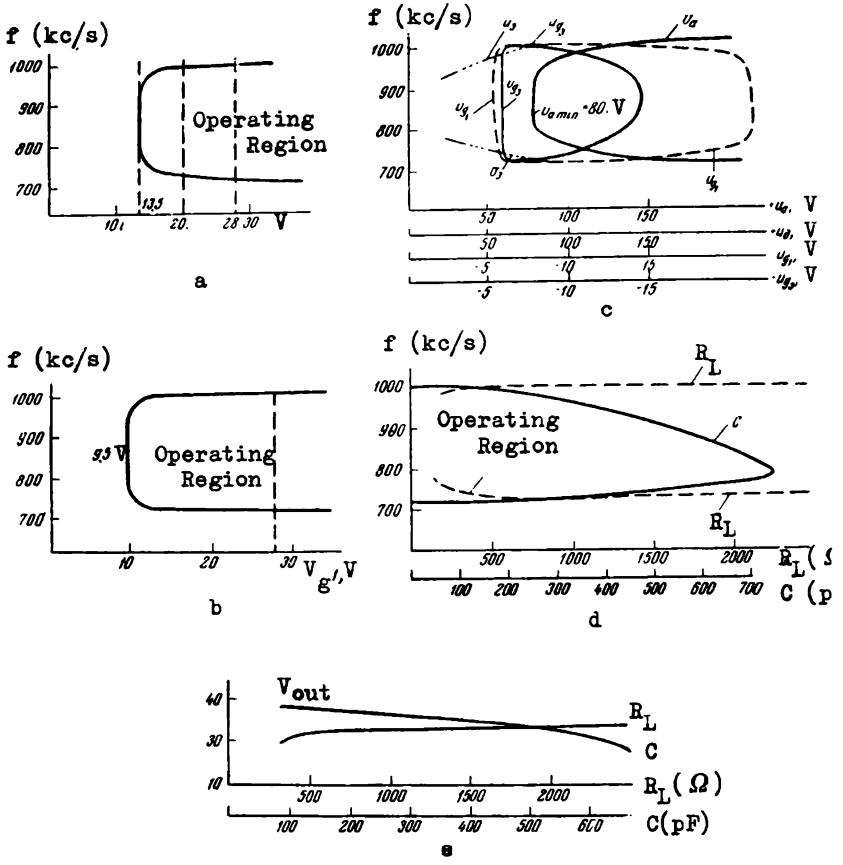

Fig. 5 Averaged basic characteristics of circuit in Fig. 2. a) Dependence of range of operational frequency f on magnitude of clock pulses, the other ratings being maintained b) dependence of range of operational frequency on value of S1 pulses, the other ratings being maintained c) dependence of the range of operational frequency on change of supply voltage d) dependence of range of operational frequency on variation of load, all other ratings being maintained e) load characteristic of a dynamic flip-flop with a delay line.

pulse causes the gates of the shift circuit to operate, instead of the coincidence gates of the flip-flops. When this happens, a code 1 held in any flip-flop is transferred through one of these gates to the next digit place.

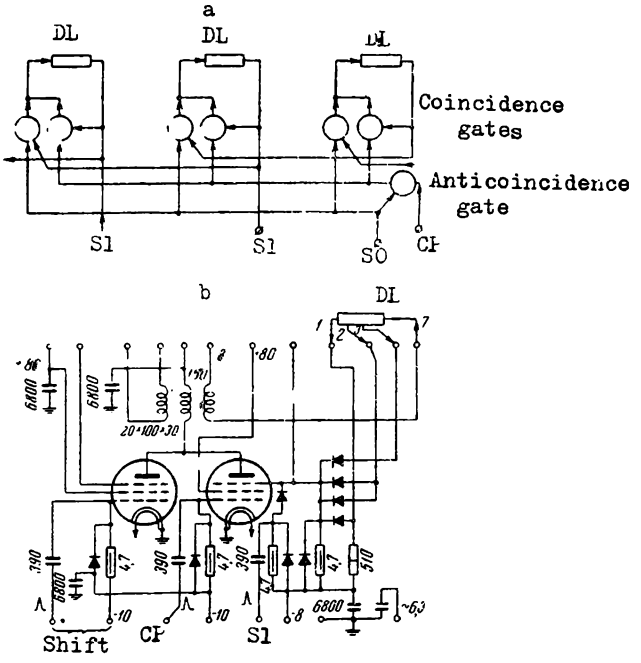

Fig. 6. Register with dynamic flip-flops. a) block scheme of dynamic flip-flop register for storing and shifting codes of numbers; b) circuit of one digit place of the register.

If a digit place holds code 0, the gate in the next digit place inhibits the pulse, and code 0 is held in it. In this way each SO pulse shifts the code in the register by one place. Fig. 6b shows the circuit of one digit place of a register constructed with the flip-flop discussed above.

If we compare the circuit shown in Fig. 6 with a normal

trigger circuit, it is immediately clear that the dynamic flip-flop is much simpler and more compact. It can in fact be four or five times smaller. A dynamic flip-flop register has the same advantages and disadvantages as the dynamic flip-flop considered in isolation.

Fig. 7 shows the main characteristics of a 7-digit place register, plotted against clock pulse frequency. Its characteristics, as we see, correspond to the characteristics of the dynamic flip-flops shown in Fig. 5.

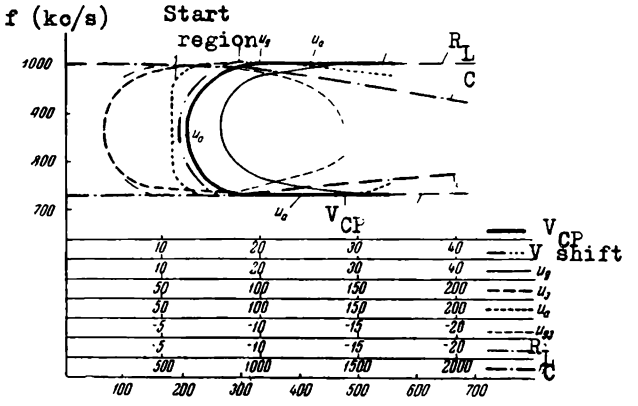

Fig. 7. Main characteristics of a register formed from dynamic flip-flops.

The type of dynamic flip-flop analyzed above is not altogether convenient, as it has a delay line which, compared with the other components, is clumsy. For this reason we have considered the possibility of replacing this delay by other less bulky components. Two variants of the dynamic flip-flop have been worked out; one with a shaping line (Fig. 8) and the other with a shortened delay line (Fig. 9). These dynamic flip-flops have characteristics similar to those of the flip-flop described above. The shaping line of the flip-flop in Fig. 8 is constructed from three miniature coils and three capacitors type KTK-11, so its size is no more than 2 cm^3. The shaping line is composed of three loops in series, with impedances as follows:

$$\varphi_1 = \frac{\pi R}{4}; \quad \varphi_2 = \frac{\pi R}{4} \cdot 3; \quad \varphi_3 = \frac{\pi R}{4} \cdot 5.$$

where R is 1.0k Ω.

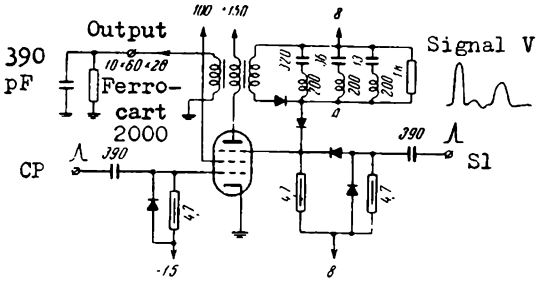

Fig. 8. Dynamic flip-flop with shaping line.

The natural frequencies of the loops are in the ratio $1 : \frac{1}{3} : \frac{1}{5}$. The inductance of all the loops is the same, and equal to 200 μH, and the capacitances accordingly are equal to 320, 36, and 13 pF. When the valve conducts, the loops are energized, and a certain number of cycles of oscillation take place, corresponding to the frequency. These oscillations, superimposed on each other, produce at the input of the shaping line the voltage waveform shown. After 0.8 to 0.9 μsec after this pulse, a similar pulse with about 2/3 the amplitude is formed; that is, it is as if a repeated signal were supplied from a delay line, but with a 1/3 attenuation. The repeated signal acts upon the suppressor grid of the valve at the moment of arrival of the next clock pulse. When this happens, the valve conducts, and a positive signal is sent from the transformer to the suppressor grid, amplifying the repeated pulse to the value of the original signal. Thus, in this type of flip-flop, thanks to positive feedback to the suppressor grid, attenuation in the line is compensated for. Therefore this system gives much greater amplification, or, in other words, has better shaping properties, which cannot but affect the reliability of working of the system. The shaping line has an impedance of about 1.0k Ω that is, twice the impedance of the delay line used in the flip-flop examined above.

The circuit for a dynamic flip-flop with a shortened delay line (Fig. 9) is almost the same as that for a flip-flop with a shaping line. A delay line of 0.3 to 0.4 μ sec is substituted for the shaping line. A signal from the secondary winding of the transformer is applied simultaneously to the suppressor grid of the valve and to the

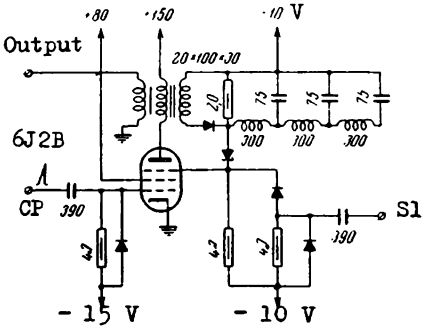

Fig. 9. Dynamic flip-flop with a shortened delay line.

delay line. In consequence, a repeat signal is reflected from the end of the delay line. The parameters of the delay line are so selected that the reflected signal is appreciably widened. Its magnitude is 2/3 the amplitude of the original pulse. It has proved possible to make the delay line of three sections. The inductance of the coils is 300 μH, capacitance 75pF, and impedance 2.0 k Ω. The delay line has the same dimensions as the shaping line.

This flip-flop has the same advantages as the flip-flop with the shaping line. Moreover, in this circuit it is much easier to widen the repeated signal: the same method of widening can be used here as in the first flip-flop. The delay line is much simpler to instal and adjust than the shaping line. Therefore, of all the circuits of dynamic flip-flops examined above, the nearest to the ideal is the circuit with the shortened delay line.

Finally, let us consider yet one more type of dynamic flip-flop (Fig. 10). This circuit is of the type shown in Fig. 1a. The circuit shown was not designed for a

register, but as a circuit playing a variety of roles in a dynamic unit. This system can be conveniently used as a dynamic flip-flop where an SO pulse is required to be applied to one or two flip-flops only. The coincidence

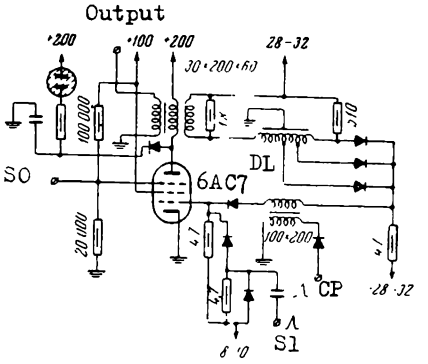

Fig. 10. Dynamic flip-flop with a delay line.

gate is constructed from a transformer and a germanium diode. The gate works on the principle of addition of signals. A single signal cannot pass the diode to the grid. A signal passes to the grid only when pulses are sent simultaneously to both inputs of the gate. The delay line is of the same type as in the first variant of the flip-flop. The widening of the signal is the standard one.

A 6AC7 valve is used here as the shaping element. It operates like an amplifier. This flip-flop, however, is not set at 0 by inhibiting a clock pulse, as in the other examples, but by applying a negative pulse to the suppressor grid. The valve then operates as an anti-coincidence gate. The anode circuit includes a neon lamp for showing the state of the flip-flop. When the flip-flop is in position 1 the capacitor in the neon lamp circuit is charged and the lamp lights; but in the intervals between pulses the capacitor discharges across the high resistance of the neon lamp.

This kind of flip-flop can provide a large output. The circuit can work with a load of 50 to 60 Ω and 7500 to 10,000 pF. Short-circuiting the secondary winding of

the flip-flop does not upset the working of the system (the transformer has leakage fluxes). The range of operational frequency is 760 to 900 kc/s. The circuit requires S1 pulses of 15 to 40 V, S0 pulses from 25 to 50 V, and clock pulses from 15 to 22 V (pulses of more than 22 V are brought within limits by the diode circuits before being applied to the flip-flop).

This circuit can be put to various uses in machines with serial action, as a dynamic flip-flop, or a shaping element, or a coincidence or anti-coincidence gate.

2. Flip-flops with Storage Capacitance

As we have already observed, the main disadvantage of the circuits we have considered is the necessity for exact coincidence of the input signals. This agreement can seriously complicate the circuits of counters and control units of parallel action machines using dynamic flip-flops with delay lines.

We consider below pulsed units for code storage (dynamic flip-flops with storage capacitance) which do not require coincidence of input signals. In using these units in combination with diode coincidence and anti-coincidence circuits, it is very easy to secure coincidence of signals at the inputs of the coincidence and anti-coincidence circuits. Dynamic flip-flops with storage capacitance have the same advantages as circuits with pulsed coupling. The absence of the requirement of coincidence of input pulses permits such systems to be used successfully in machines with parallel action.

The operation of a flip-flop with storage capacitance is based on the well-known principle of rapid charging of a capacitor through a low resistance, and slow discharge through a high one.

Such a circuit resembles the dynamic flip-flop with a delay line in its principle of operation. Like the delay line dynamic flip-flop, this circuit continuously puts out pulses synchronous with the clock pulses while the circuit is in position 1. When the circuit is in position 0, no pulses appear at the output. The circuit is triggered into one or other position by pulses applied to its two inputs. A positive pulse S1 applied to one input triggers the circuit into position 1, and a negative pulse S0 applied to the other input sets it in position 0.

We shall consider below three variant systems (Figs. 11a, b, c). In Fig. 11a clock pulses of positive polarity and with a frequency of 1.0 mc/s are applied to the control grid, and in 11b and 11c clock pulses of negative polarity and with a frequency of 500 kc/s are applied to the cathode.* In the last two systems the clock pulses originate in impulsers having one terminal of their output windings earthed. These pulses are limited by junction diodes to -18 V.

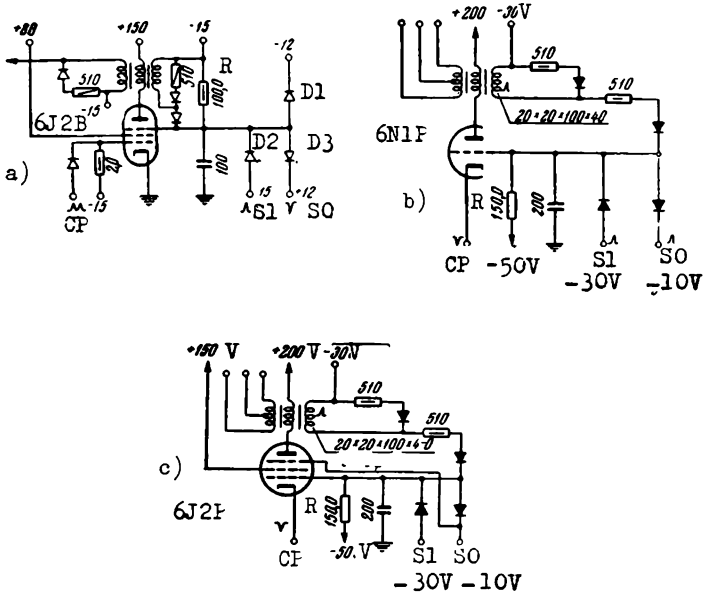

Fig. 11. Dynamic flip-flops with storage capacitance.

*The frequency of the clock pulses is chosen to correspond to the operating conditions of the units in which these flip-flops are used. In the last two a frequency of 500 kc/s is indicated, as certain other elements of the machine work at a lower speed, limiting the speed of the machine as a whole.

S1 pulses are supplied from the output windings of the transformers of similar flip-flops or of other circuits with a similar output. These output windings have a constant voltage level of -12 V in the first circuit and -30 V in the other two.

S0 pulses are supplied by similar impulsers, but the output windings of these impulsers have a constant level of +12 V in the first system and -10 V in the last two.

S1 input pulses charge the capacitors of the flip-flops through the low forward resistances of the diodes. Charging the capacitors takes very little time; it is accomplished substantially during the rise time of the pulse. In the intervals between pulses the charged capacitors discharge slowly through high resistances. When the capacitors are charged, the valves provide a path for the clock pulses, which, passing through the valves and the feedback windings, regenerate the lost charge in the capacitors. This regeneration continues until negative S0 pulses are applied, which quickly discharge the capacitors. The valves then cease to transmit clock pulses.

The resistance R, equal to 100 k Ω in Fig. 11a and to 150 k Ω in Figs. 11b and c, maintains a low voltage across the capacitors (-11 V in 11a, and -30 V in 11b) when the flip-flop is in zero position. In order to exclude the influence of the back resistance of the diodes completely under this condition, in the circuits shown in 11b and c the resistance R is connected to a supplementary power supply of -50 V, and resistances of 510 Ω and diodes connected in parallel with the output windings extinguish transients in the transformer. Resistance in the feedback circuits in the last two flip-flops serves to reduce the feedback.

The flip-flop circuit with storage capacitance shown in Fig. 11a has the following nominal ratings: anode voltage 150 V; screen grid voltage 80 V; bias on control grid and suppressor grid 15 V; transformer with Ferrocart 1000 core with the following dimensions: external diameter 7 mm, internal diameter 4 mm, thickness 2 mm; primary 100 turns, secondary 40 turns, feedback winding 40 turns.

The range of operating frequency for this system is wide. However, during the investigation it was limited by the working range of the clock pulse generator, and was 350 - 1150 kc/s.

The circuit permits considerable departures from the nominal ratings. For instance, with a clock pulse frequency of 1000 kc/s, the following departures of one of the parameters are permissible, with all other parameters at their nominal ratings: V_a(min) 80 V; V_{g2} 20 to 100 V; V_{g1} 17 V; V_{S0} 0 to 60 V; V_{S1} 17 V.

Peaky working pulses with a basic duration of 0.3 to 0.4 μsec; S1(min) 10 V (the upper limit is not restricted); clock pulses, min. 12 V, max. 30 to 35 V (restricted by the value of the dissipation rating of the screen grid).

Fig. 12 shows the load characteristic of the flip-flop in Fig. 11a, and Fig. 13 shows oscillograms of the voltages at different points in the circuit.

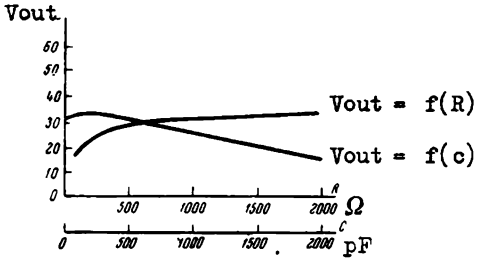

Fig. 12 Load characteristic of flip-flop in Fig. 11a.

The circuit shown in Fig. 11b has the following nominal ratings: V_a-200 V; V_{S1}-30 V; V_{S0}-10 V; V_R-50 V. Transformer with Ferrocart core (Ferrocart 200C). External diameter 7 mm, internal diameter 4 mm, thickness 3 mm; W_1 = 100 (primary winding); W_2 = 20 and W_3 = 40 (secondary windings). R = 150 kΩ. C = 150 pF. Frequency range 100 to 1350 kc/s. Clock pulses peaky, clipped, with amplitude of 20 V, basic duration 0.4 to 0.5 μsec. S1 and S0 pulses peaky, with amplitude of 25 V and basic duration 0.4 to 0.5 μsec.

The flip-flop circuit with a triode (Fig. 11b) permits the following departures of parameters from the nominal ratings (all other parameters being at the nominal ratings):

V_a 100 to 300 V; V_{S1} - 27 to -34 V; V_{SO} -6 to -17 V;
V_R -36 to -100 V; $S1_{min}$ 10 V; SO_{min} 15 V.

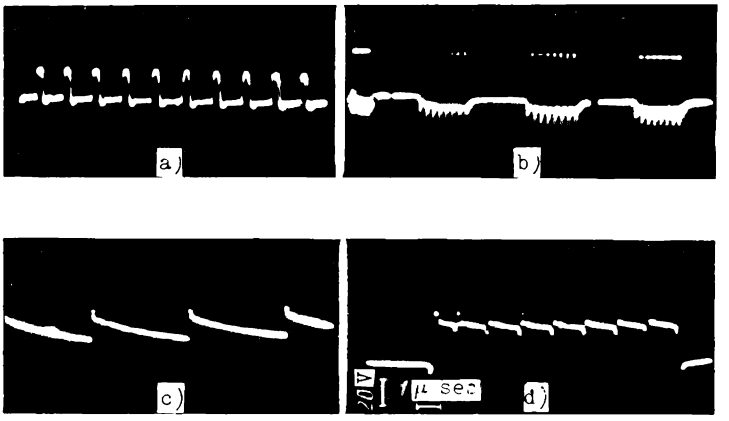

Fig. 13. Oscillograms of pulses at different points of flip-flop in Fig. 11a a) clock pulses b) output pulses c) voltage in capacitance without regeneration of charge d) voltage in capacitance in normal working. The horizontal and vertical lines indicate 1 μsec and 20 V respectively.

Fig. 14a shows the load characteristics of this flip-flop. Fig. 14b gives the curve of the change of value of the output pulse in the output winding of the transformer ($W = 20$), depending on the frequency of succession of the clock pulses. It also shows the change of the initial voltage level in the output winding in relation to the frequency of succession of the clock pulses. Both characteristics were taken with a load $R = 1\ k\Omega$.

The basic data of the third variant of the flip-flop (Fig. 11c) are the same as for the second. The load characteristic of this flip-flop is shown in Fig. 15. The characteristics in Fig. 14b are approximately the same for this flip-flop.

Unlike dynamic flip-flops with a delay line, these circuits do not require coincidence of input signals with

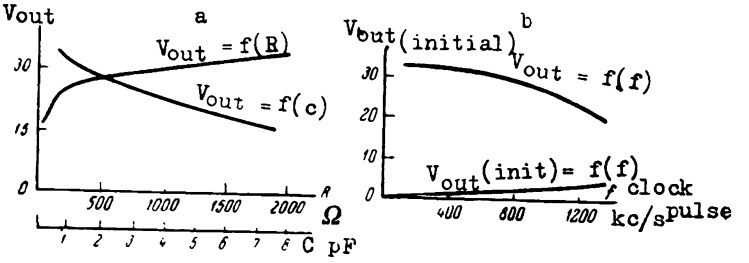

Fig. 14. Basic characteristics of circuit shown in Fig. 11b a) load characteristic b) frequency characteristic.

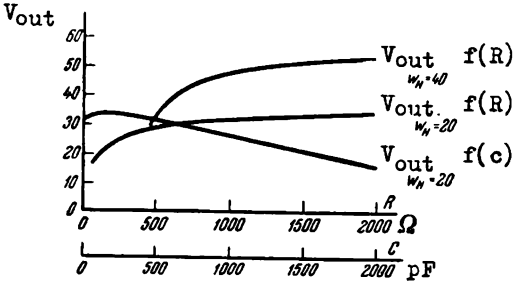

Fig. 15. Load characteristic of dynamic flip-flop as in Fig. 11c.

clock pulses. The systems work correctly, no matter when the input pulses are supplied. It is true that for the first two types it is better that the SO pulses should not coincide with the clock pulses, since their effect on the capacitance is opposite. Where this may happen, it is better to use the circuit of Fig. 11c, as in this system the arrival of an SO pulse is not restricted in time, because this pulse is blocked by the clock pulses. Output of code from dynamic flip-flops takes place at the moment of action of the clock pulses.

However, we can also realize the output of codes at arbitrary times with the aid of these systems. In order to do this, the grids of the valves of two dynamic flip-flops

are connected. The storage capacitance of only one flip-flop is used; the storage capacitance of the other is disconnected. Clock pulses are supplied to one flip-flop, as usual, but to the clock pulse input of the other a code output signal is applied. This signal passes through the valve of the second flip-flop, if the first is in position 1. Thus the second flip-flop here plays the part of a pulsed-potential coincidence circuit.

The dynamic flip-flop circuit with storage capacitance can operate on an element registering signals sent out of phase, such as that shown in Fig. 16, which will be discussed later. There will be a pulse at the output of the system if pulses are applied to both inputs. The sequence of these pulses must be completely determined: first an S1 pulse, then a pulse at the clock signal input. It is best to supply the pulse which has reached the output through a short delay line, to the S0 input, so that the system shall return quickly to its initial state. This adaptation of the dynamic flip-flop easily secures synchronization of signals delayed for various lengths of time in passing through various logical elements, at the inputs of the diode coincidence and anti-coincidence circuits in parallel action units.

Dynamic flip-flops of the types here considered can also be used as ordinary pulsed amplifiers and as pulsed coincidence and anticoincidence circuits. To this end we must provide for the possibility of disconnecting the capacitors from the valve grid. In this way the number of different types of element in the circuits of a machine using dynamic flip-flops can be considerably reduced.

Dynamic flip-flops with storage capacitance not only retain all the virtues of dynamic flip-flops with delay lines, but have also a whole series of advantages over them.

1) The dynamic flip-flop with storage capacitance has no delay line. By comparison with the other components of the circuit, the delay line is the bulkiest element; therefore the dynamic flip-flop with storage capacitance is more compact.

2) The absence of a delay line, which has a restricted pass-band, renders the system uncritical to the shape of the output and input signals.

3) The admissible range of variation of frequency of

clock pulses for a dynamic flip-flop with storage capacitance is much greater than that for dynamic flip-flops with delay lines.

4) The minimum frequency of clock pulses for the dynamic flip-flops here described is seven times less than the operating frequency of these pulses. Therefore loss or abrupt change of several clock pulses does not involve dislocation of the system, whereas loss or abrupt diminution of only one clock pulse in the circuit of a dynamic flip-flop with a delay line does involve this. Therefore the dynamic flip-flop with storage capacitance (especially that in Fig. 11a) is considerably more stable in the event of variation of clock pulses.

5) Finally, the chief advantage of the dynamic flip-flop with storage capacitance is that this system does not require coincidence of input signals and clock pulses, whereas in the circuit of a dynamic flip-flop with a delay line this is obligatory. Therefore the possible applications of the dynamic flip-flop with storage capacitance are considerably wider than for the flip-flop with a delay line.

Since the dynamic flip-flop with storage capacitance does not require coincidence of input signals, and can be used as a pulsed-potential coincidence circuit, and also as a matching unit at the inputs of diode logical elements, it is possible to use it in the most various counting and controlling units with parallel action. The dynamic flip-flop with storage capacitance permits the coupling between elements of these units to be pulsed in most instances. Besides this, dynamic flip-flops with storage capacitance, as we shall see below, make it possible to carry out a whole series of operations in these units asynchronously with the clock pulses. In systems carrying out such operations, the clock pulses are, in fact, an auxiliary source of power supply, by means of which position 1 of the dynamic flip-flop can be maintained indefinitely. The highest operating frequency of the flip-flops in these systems is determined only by the minimum admissible interval between S0 and S1 pulses. This interval is, for the flip-flops here described, 0.2 μ sec, which corresponds to a greatest admissible frequency of operation of the flip-flop of 5 Mc/s.

Thus, systems with dynamic flip-flops with storage capacitance can work at a frequency much higher than that of the clock pulses.

3. Units with Parallel Action using Dynamic Flip-flops with Storage Capacitance

To obtain a complete idea of the circuits of parallel-action machines constructed with dynamic flip-flops with storage capacitance, it is enough to examine systems which carry out the following six elementary operations:

1) setting the digits of a block (or of individual storage units) at 0;

2) receiving code in the register (or in individual storage units);

3) output of code from the register (or from individual storage units);

4) inversion of codes (for instance, to inverse code);

5) shift of codes in the digit places of the register;

6) elementary addition of codes.

Execution of all arithmetical and logical operations by elements of the arithmetic unit reduces to these operations. Therefore the arithmetic unit consists, basically, of circuits carrying out these operations. The majority of elements of the control unit consists of analogous circuits. It is true that systems carrying out the connexion of one or another output circuit, depending on the combination of codes acting on their inputs, are also characteristic of control systems. We shall consider the working of this kind of system, using as an example the dynamic decoder.

Elementary operations of output and receipt of codes by registers in a parallel-action machine. Fig. 16 shows three registers synchronized by pulses differing in phase, and the circuits for receipt and output of codes.

Fig. 17b gives details of the output coincidence gates, B1, B2, B3, of Fig. 16. Positive signals Bp1, Bp2, Bp3 are applied to the inputs of the gates from impulsers connected to a d.c. voltage source of -30 V. This system can be used as an anti-coincidence gate. In this case, besides positive working pulses supplied to the inputs of the gate at a voltage level of -30 V, negative blocking pulses at a voltage level of -10 V are applied to one of the inputs.

Fig. 17a shows the circuit of each input gate B of Fig. 16. The fairly powerful transformer output is able to

energize the inputs of the dynamic flip-flop directly.

Let us suppose that it is required to transfer the contents of register R1 to R2. In this case the signals

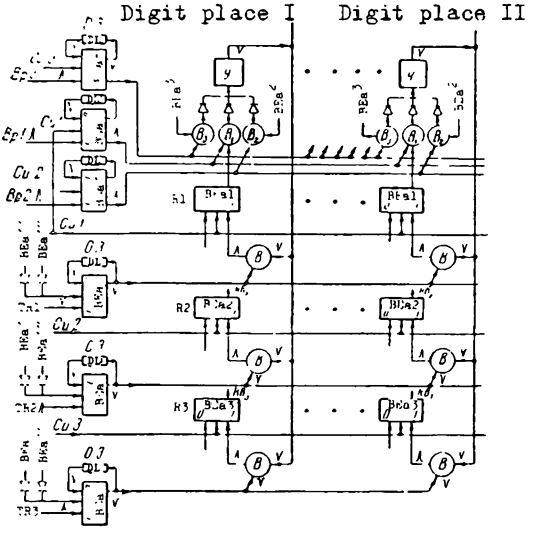

Fig. 16. Circuits for receipt and output of the codes of three registers synchronized by pulses different in phase.

Bpl (from register 1) and TR2 (to register 2) are applied from the signal control circuit to the flip-flops controlling the output gates of R1 and the input gates of R2. These signals trigger the corresponding flip-flops into position 1. The pulses Bpl and TR2 are not synchronous with the clock pulses of the first register, so at the initial moment there is no output from the register. The contents of the register are transferred only when the clock pulses Cul occur. The first clock pulse after Bpl passes through the flip-flop BEa' and energizes the inputs of the output gates Bl*. At this moment there

*By BEa (basic element type "a") we shall denote a dynamic flip-flop with storage capacitance consisting of a valve 6N3P and by BEb a flip-flop with valve 6J2P.

are pulses at the second inputs of the gates Bl of the digit places in position 1. So the gates in these digit places send pulses to the input gates of register R2. In those digit places of register Rl which contain 0, the gates Bl do not let pulses pass to the output.

Transfer of its contents from register Rl on the signal Bpl takes place once only, because of the introduction of feedback from the output of BEa' to its SO input. The first clock pulse passing through BEa' opens a passage for the following Cul pulses.

BEa' also energizes the clock pulse inputs of the flip-flops controlling the input circuits of registers R2 and R3. In the present case the flip-flop controlling the inputs of register R2 is open to a pulse from BEa'. This pulse passes through to the inputs of the gates of R2 at the instant that pulses from the Bl gates arrive at the other inputs. In the digit places to which pulses are supplied from the Bl gates, the input gates of R2 pass signals to the Sl inputs of the corresponding flip-flops.

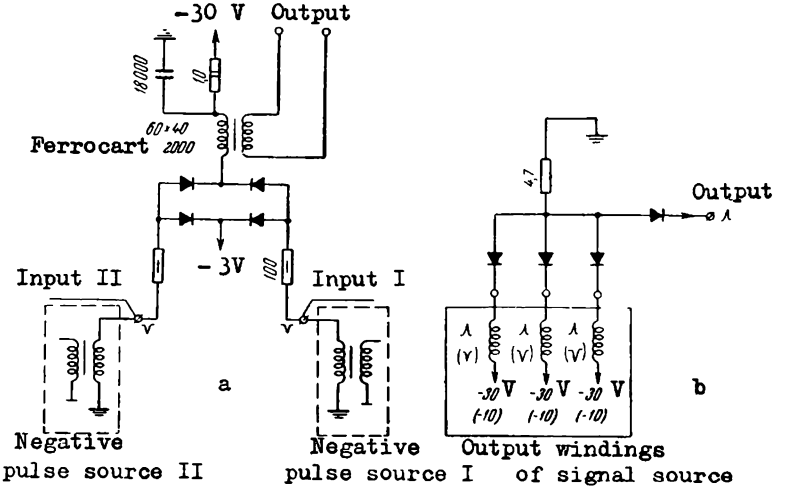

Fig. 17. Circuits of diode coincidence gates a) gate with transformer output b) gate with resistance.

In the digit places to which zeros are applied from Rl, the input gates of R2 exclude the pulses. The corresponding flip-flops remain in position 0. In this way

the codes from R1 are set in R2. This takes place synchronously with the clock pulses Cul. The flip-flop controlling the input gates of R2 is set to position 0 by a pulse from its own output.

Reception and output of codes is carried out in the same way by the other registers. In the circuit in question, as we see, there is no need to be concerned about coincidence of signals at gate inputs, as this is always secured. The necessity for control signals to be in phase with clock pulses, which is characteristic of other systems with pulsed coupling, disappears. Transfer of codes takes place independently of the arrival of control signals, at the instant of arrival of clock pulses at the register which is putting out codes.

A number can be put out from a register in inverse code. To do this, the output coincidence gates must be replaced by anti-coincidence gates. Negative pulses are applied to the controlling inputs of the gates from the flip-flops of the corresponding digit places, and positive pulses to the operating inputs are supplied from the flip-flop controlling the output circuits. It is obvious that positive pulses pass to the outputs of gates in those digit places where there are no negative pulses; that is, those holding code 0. Thus the pulses at the outputs of the gates correspond to the inverse code of the number to be transferred.

Fig. 18 shows oscillograms of the voltages at the inputs and output of the gate giving out codes. Fig. 19 shows oscillograms of the signals at the inputs and output of the input gate.

Shift. Fig. 20a shows circuits for carrying out unsynchronized shift of codes held by flip-flops in a BEa register. In this circuit a shift pulse can arrive at any time with respect to the clock pulses. A shift pulse is amplified in power by the shaper ϕ_3, and energizes the pulsed-potential gates of all the digit places y_5*,

*The shapers ϕ_2, ϕ_3, the pulsed-potential gates y_5, and the amplifiers, are connected (on the basis of the dynamic flip-flops described above) to a triode. The capacitance of these flip-flops is disconnected from the valve circuit, and instead either a circuit with amplified signals (in ϕ_2, ϕ_3, and y_5) or the capacitance of a BEa flip-flop (in gates y_5) is connected.

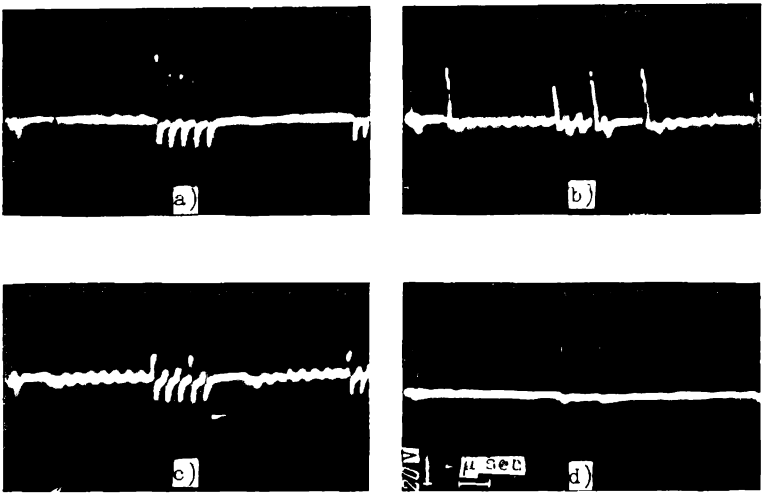

Fig. 18.1 Oscillograms of voltages at different points of the output gate of one of the 45 digit places of a register. All gates from one input are controlled from one shaper (the most difficult case; noise can in this case have maximum value; this happens when the flip-flops of all digits are in position 1; this is recorded in some parts of the photographs). a) pulses at the flip-flop output b) pulses at the output of the common shaper c) pulse at the output of the gate d) pulses after the amplifier. Scales of 20 V and 4 μsec are shown.

and also the diode shift gates B (Fig. 17b), controlled from the other inputs of the pulsed-potential gates y_5. In those digit places holding code 1 the shift pulse passes through the pulsed-potential gates. Therefore in these digit places the gates B send out pulses to the delay lines connected to the S1 inputs of the flip-flops of the next digit places.

After pulses are sent from the gates B to the delay lines, all flip-flops of the register are set in position 0. The flip-flops of the register are cleared by shift pulses passing with a delay of 0.2 μsec.

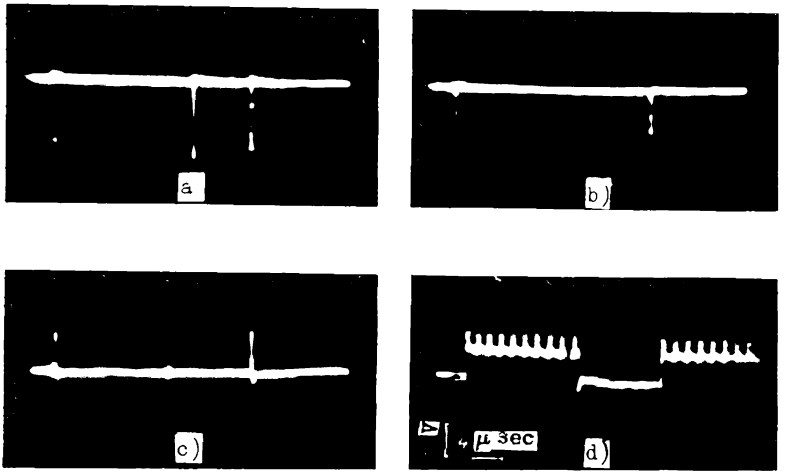

Fig. 19. Oscillograms of pulses at the inputs and output of a transformer gate a) pulses at one of the inputs b) pulses at the other input c) voltage at the output of a gate connected to the S1 input of a flip-flop d) voltage in the circuit of a flip-flop triggered by the gate. Scales of 20 V and 4 μsec are shown.

After the BEa flip-flops are set in position 0, pulses are sent from the delay line. These pulses arrive at the digit places which follow digit places holding code 1. They set the flip-flops in position 1, and code 1 is carried one digit place.

In digit places holding zero, the pulsed-potential gates have not sent signals to the gates B, so there have been no pulses there or in the delay lines. Flip-flops connected to these delays have remained in position 1 after the clearing pulse. So we can take it that code 0 has been transferred to the next digit place.

As we can see from the diagram, the shift circuits are completely disconnected from the clock pulses. Therefore a shift pulse can occur at any time, at a frequency bearing no relation to the frequency of the clock pulses CP.

It may happen that clearing pulses coincide with clock

pulses, which is undesirable, as these pulses energize the capacitance in different ways. To avoid this, clock pulses are blocked in the anti-coincidence gate Ga by SO pulses.

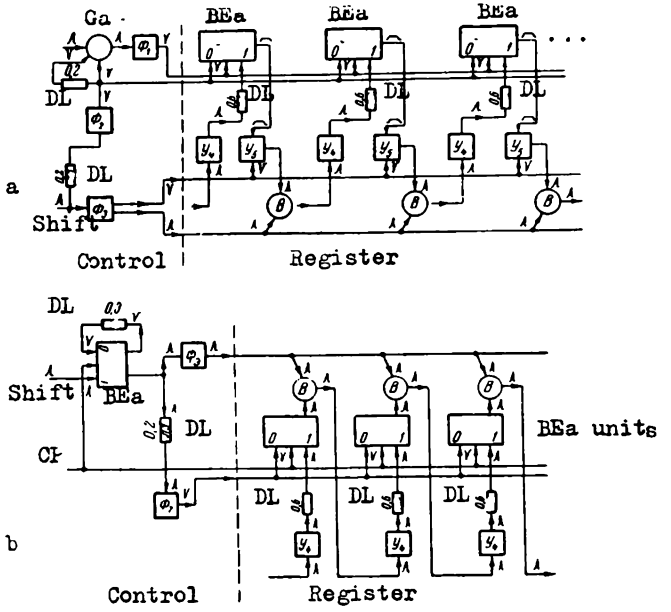

Fig. 20. Shift circuits a) for producing unsynchronized shift b) for producing synchronized shift.

In this kind of register, clock pulses act only as signals supplying the system with power. They play no part in the carrying out of the operation, and serve only to maintain the state of the flip-flops.

Let us now consider the register with circuits for bringing about synchronized shift (Fig. 20b). The circuit is similar, but without the pulsed-potential gates. The shift gates (B) are directly controlled by flip-flops. This circuit operates like the other. Signals from the inputs of the gates B always coincide, thanks to the matching flip-flop BEa. This flip-flop works in exactly the same way as BEa' in the circuit for the output of

codes (Fig. 16). Shift pulses in this system need not be in phase with the clock pulses. However, the source of these pulses must be started across various intervening circuits by the same pulse generator that starts the clock pulses.

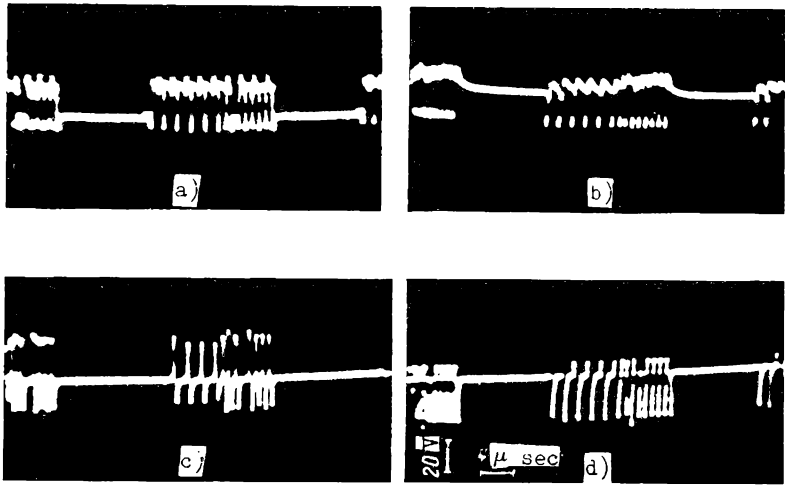

Fig. 21. Oscillograms of voltage at various points in unsynchronized shift circuits a) in the capacitance of the flip-flop of one of the digit places b) shift pulses at the inputs of pulsed-potential gates c) pulses at the output of pulsed-potential gates of one of the digit places d) pulses at the output of a diode gate. Scales of 20 V and 4 μsec are shown.

The register with unsynchronized shift circuits has one and a half valves per digit place. We have investigated the possibility of triggering the flip-flops from the gates of the transformers (Fig. 17a) across a delay line with impedance of 500 and 1000 Ω. Pulses were sent to the gate inputs from flip-flops and shapers. The pulses at the inputs to the flip-flops were sufficiently powerful, after the delay lines, to trigger the flip-flops (15 to 22 V). Especially significant results were obtained with delay lines having an impedance of 1.0 kΩ. In this way a register with synchronized shift circuits can be constructed, using only gates and delay lines in

the shift circuits. Nevertheless, an unsynchronized shift system is preferable for universal machines, as it is more flexible. The unsynchronized shift circuit can carry out shifts at a far higher frequency than that of the clock pulses. Pulsed-potential gates and amplifiers can be used for the operations of code inversion and addition. In the more complicated registers, in which, besides shift, code inversion and addition are carried out, the economy in equipment as compared with synchronized shift circuits is inconsiderable.

Fig. 21 illustrates unsynchronized shift. The oscillograms were taken when a register in position 0 received the code 11111011111. The frequency of shift is first 500 kc/s, then 1 Mc/s, and the frequency of the clock pulses of the register is 500 kc/s.

Code Inversion. Circuits for carrying out the operation of code inversion are almost the same as those for shift, only here, instead of the coincidence gates B (Fig. 20), there are anti-coincidence gates Ga and delay lines connected not to the following digit place but to the same one. Negative control pulses arrive at the gates from the pulsed-potential gates (Fig. 20a), or from the flip-flops themselves (Fig. 20b), and positive operational signals arrive from the shaper ϕ_3. A pulse from ϕ_3 passes the gates of those digit places where there are no negative signals blocking the gates; that is, which hold code 0. Pulses at the outputs of the gates of these digit places trigger the flip-flops, across delay lines, into position 1. In the digit places holding code 1 no pulses are formed at the output of the anticoincidence gates, and the flip-flops remain in position 0 after the clearing pulses. In this way, as a result of one inverting pulse, the inverse code of the number is formed in the register.

Addition. Fig. 22 shows a circuit for unsynchronized addition. Let us suppose that the codes of the first term are held in the flip-flops BEb of the adder. Then at any moment of time the codes of the second term are supplied to the adder simultaneously in all digit places from the output circuits of the register (we have already considered the output of the contents of the register).

Let us consider the case when a further unit is added to a unit in a given digit place (1+ 1 = 0 and carry). The pulsed-potential gate U_2 is in this case open to an

input signal.* The carry pulse originates at the output of gate U_2. An input signal also passes through the delay line and confirms the flip-flop in state 1. At

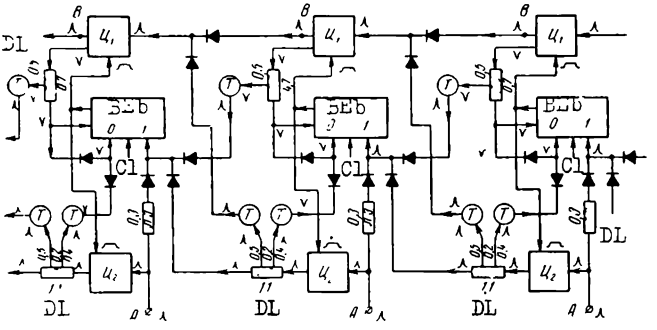

Fig. 22. Circuit for unsynchronized addition.

the same time a pulse from gate U_2 passes a section of the delay line in 0.4 μsec and sets the flip-flop at 0 across the transformer. The setting at 0 follows immediately upon the end of a pulse at the Sl input.

Now let us consider the case when the flip-flop of a given digit place is in position 0, and 1 is added to it (0 + 1 = 1, no carry). In this case no input pulse passes gate U_2, and no carry pulse is formed at the output of the gate. 0.3 μsec after the start of the input pulse, the flip-flop is set in position 1. A delay of 0.3 μ sec does not enable the input pulse to pass through gate U_2, as the flip-flop controlling this gate only begins to operate after the pulse at the input of the gate is finished.

Let us now turn to the digit place in which a carry pulse is formed. While the carry pulse from the output

*The pulsed-potential gates U_1 and U_2 are based on flip-flops with a 6J2P valve. The suppressor grids are connected to the capacitances of the BEb valves. Operating signals are supplied to the control grids.

of gate U_2 passes through sections of the delay line in 0.4 and 0.2 μsec, the flip-flops are set by the input pulses in position 1 or 0. The carry pulse, passing through these sections, is applied to carry circuits of similar construction to the input circuits already examined. In these, instead of the gate U_2, there is a gate U_1, instead of a delay line of 0.3 μsec there is a section of delay line of 0.5 μsec, and instead of a section of delay line of 0.4 μsec connected to the output of gate U_2, there is a delay line of 0.7 μsec connected to the output of gate U_1. If the flip-flop of the next digit place is in position 1, the carry pulse passes through gate U_1, and after a delay of 0.7 μsec triggers the flip-flop of this digit place into position 0.

If the flip-flop is in position 0, the carry pulse does not pass through gate U_1, but after a delay of 0.5 μsec it triggers the flip-flop of the next digit place into position 1. Since the pulses are widened in passing through the delay lines, in this circuit the delay lines are a little longer: 0.5 μsec instead of 0.3; and 0.7 instead of 0.4.

Carry pulses from gate U_1 are applied not only to the S0 inputs of their digit places, but also to the digits following. The inputs to the digits following, for carry pulses from gates U_1, form the system considered earlier. In them also a section of delay line of 0.5 μsec leads to the S1 input of the next digit place, and from the pulsed-potential gate U_1 a delay of 0.7 μsec is connected to the S0 input of the flip-flop.

In this way carry pulses can be sent to the digits following from either U_1 or U_2. If a pulse is sent by gate U_1, there can be no signal at the U_2 output of the given digit place. Likewise when a pulse is sent from U_2, no signal is possible from U_1.

The pulsed-potential gates U_1 form a consecutive chain of carry-through along all the digit places of the adder.

If all the digit places are in position 1, and 1 is added to the lowest digit, a through carry is made by the carry chain U_1. The carry pulse, traversing the elements of the chain U_1, triggers the flip-flops of these digits into position 0, and continues along the chain until it meets on the way a digit place holding code 0. In the most adverse case, the carry pulse can pass through n - 1 digit places of the adder (n being the full number of digit places).

If we remove from the adder circuit (Fig. 22) the pulsed-potential gates U_2, the delay lines of 1.1 μ sec, and all circuits connected to these elements, what remains is the circuit of a binary counter. The input pulses of this system must be supplied to flip-flop B of the lowest digit place.

In the system we are considering, none of the circuits is connected to the clock pulses. For this reason codes of the terms can be supplied to the adder at any time. Since triggering of the flip-flops to 0 by carry pulses can coincide with the clock pulses, in this system flip-flops of the third type (Fig. 11c) are used. Pulses from a delay line of 0.7 μsec arrive not only at the 0 inputs, but also at the suppressor grids of the valves, interrupting for this period the passage of clock pulses. The adder circuit for carrying out unsynchronized addition contains three valves to a digit place; the counter circuit has two valves. We have investigated the circuits of adders carrying out synchronized addition. These systems required two valves to a digit place. They are not suitable for a machine with parallel action, and we shall not consider them here.

Fig. 23 shows oscillograms of the voltages in the capacitors of flip-flops of three digit places during uninterrupted supply of ones to all digit places. This case includes all possible combinations of carries in the adder.

Operation of a pulsed decoder formed from dynamic flip-flops. Fig. 24 shows the circuit of a pulsed decoder with 15 outputs, controlled by four flip-flops. Flip-flops in position 1 send positive and negative pulses to the circuit at the same time. The circuit of the decoder consists of 15 coincidence and anti-coincidence gates. Depending on the code held in the flip-flops, pulses pass

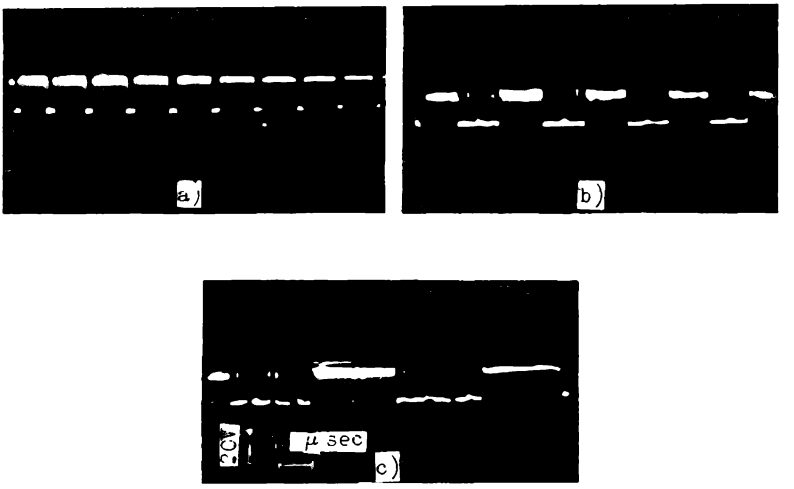

Fig. 23. Oscillograms of voltages in the capacitors of flip-flops of three digit places when 1 is fed uninterruptedly to all digit places a) voltage in the capacitor of flip-flop of the first digit place (slow scan) b) 2nd digit place c) 3rd digit place. Scales of 20 V and 10 μsec are shown.

through one or other set of gates. It is easy to see that when all the flip-flops are in position 0, none of the gates sends a pulse.

Figs. 25a and b are oscillograms of pulses at the output of a decoder working with a 4-digit counter, in two scannings of the oscilloscope. Fig. 25c is an oscillogram of pulses at one of the inputs of the same decoder.

The systems in question have a number of considerable advantages over similar systems with other kinds of storage unit, for instance, ordinary flip-flops. The systems we are considering call for a considerably smaller number of components (especially valves) than do systems with ordinary flip-flops. In high-speed systems the difference is particularly marked (3 to 4 times less).

Current flows in most of the elements of the systems we have considered only during the action of the pulses. This makes it possible to use components which are small

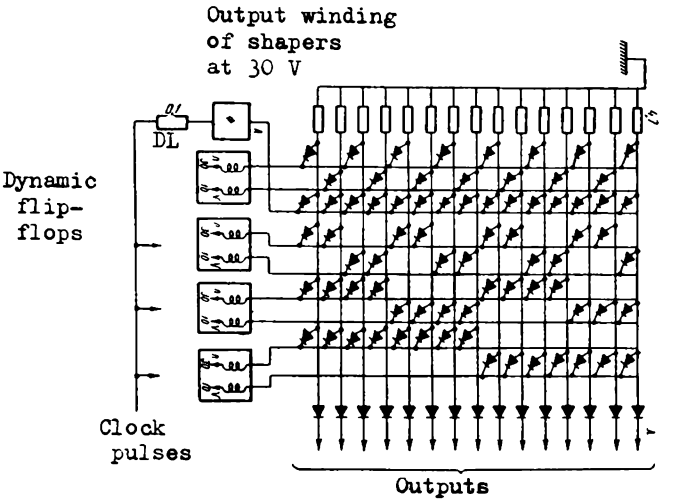

Fig. 24. Circuit of a pulsed decoder with 15 outputs, controlled by dynamic flip-flops.

both in size and power, and to reduce the dimensions of the systems. A dynamic flip-flop can be made 4 to 5 times smaller than an ordinary flip-flop.

The systems here described require little power and generate little heat. This makes it possible to dispense with ventilation in machines using these systems.

By comparison with the circuits of BESM (ordinary flip-flop cells are used as storage units in this machine) the systems here described permit considerably greater deviation from the nominal ratings of the supply voltages and operating signals. For this reason these systems are more stable in operation.

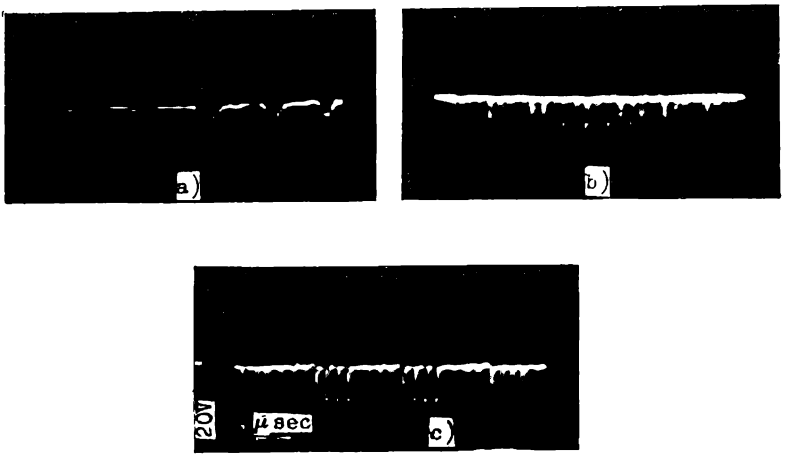

Fig. 25. Oscillograms of voltage at the input and output of a decoder a, b) voltage at one of the outputs of a pulsed decoder controlled by a counter with dynamic flip-flops (oscillograms taken in similar scans of the oscilloscope) c) pulses at one of the inputs of the decoder. Scales of 20 V and 4 sec are shown.

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VALVE TYPES

The valve type numbers quoted in this paper, with the exception of 6AC7, are transliterations of the original Soviet type numbers. The characteristics of these valves, as given in Russian-English Electronics and Physics Glossary, Consultants Bureau, New York (1957), are as follows:

6J2B (sub-miniature r.f. pentode)	V_h 6.3 V, I_h 0.2 A, V_a 120 V, V_{g2} 120 V, I_a 5.5 mA, V_{gl} −2 V, g_m 3.2 mA/V, c_{in} 4.9 pF, c_{out} 4.1 pF, c_{ag} 0.03 pF.
6N1P (bantal double triode)	V_h 6.3 V, I_h 0.6 A, V_a 250 V, R_k 600 Ω, I_a 8.0 mA per triode, g_m 3.2 mA/V, R_{in} 11 kΩ, p_a 2.0 W per triode.
6J2P (bantal r.f. pentode)	V_h 6.3 V, I_h 0.175 A, V_a 120 V, V_{g2} 120 V, R_k 200 Ω, I_a 5.0 mA, g_m 3.5 mA/V, R_{in} 75 kΩ, c_{in} 4.1 pF, c_{out} 2.2 pF, c_{ag} 0.02 pF.
6N3P (bantal double triode)	V_h 6.3 V, I_h 0.35 A, V_a 150 V, R_k 240 Ω, I_a 7.7 mA per triode, g_m 4.9 mA/V, R_{in} 7.5 kΩ, p_a 1.5 W per triode.

6AC7 This is the American equivalent of the original Soviet type.

(Editor)

E. A. VOLKOV

A METHOD OF AUTOMATIC MONITORING OF A SERIAL ARITHMETIC UNIT

In Fig. 1 we show the usual scheme for a serial (one-digit) binary adder. The codes of the summands, beginning with the least significant, are supplied to inputs I and II. The digits of the sum appear in turn at the output IV. Output V supplies the carry to the next digit by way of the delay line DL to input III of the adder.

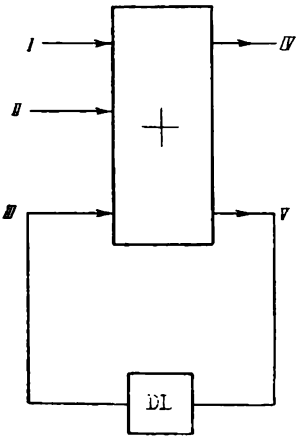

Fig. 1.

Let us examine Table 1. Under "Inputs" and "Outputs"

it gives the eight known possible combinations of signals to inputs I, II, and III, and the corresponding signals at outputs IV and V of the adder. The next three columns show the total number of units at inputs I, II, and III, the total number of units at outputs IV and V, and their difference.

TABLE 1

Inputs			Outputs		Total of units		Difference
					at inputs	at outputs	
I	II	III	IV	V	I + II + III	IV + V	(I + II + III) − (IV + V)
0	0	0	0	0	0	0	0
1	0	0	1	0	1	1	0
0	1	0	1	0	1	1	0
0	0	1	1	0	1	1	0
1	1	0	0	1	2	1	1
1	0	1	0	1	2	1	1
0	1	1	0	1	2	1	1
1	1	1	1	1	3	2	1

We shall consider the working of the adder from a rather unusual viewpoint; namely, as the conversion of a number of units supplied to inputs I, II, and III into a number of units put out at outputs IV and V. Comparing the last column of Table 1 and the column for output V, we come to the conclusion that loss of a number of units at the outputs of the adder coincides with the appearance of units at output V (the carry circuit). We can base certain rules on this conclusion.

1. In adding with a serial adder, the number of units in the summands is equal to the number of units in the sum plus the number of carries.

The second rule follows from the first.

2. The number of units in the summands and sum plus the number of carries in adding is even.

For example,

$$\begin{array}{r} 101101 \\ +\,111001 \\ \hline 1100110 \end{array} \qquad \begin{array}{r} 011011 \\ +\,010001 \\ \hline 101100 \end{array}$$

In the first example the number of units in the sum plus the number of carries is 8, in the second example 6.

Rule 2 can be used as a check on the addition of binary codes in a serial adder. We introduce a so-called monitoring flip-flop. During serial read-out of terms from the store, the monitoring flip-flop counts the number of units in the terms in pairs. Then during the addition it goes on to count the number of carries. Finally, when the sum is written, the monitoring flip-flop counts the number of units in the sum. Clearly, after the sum is written, the monitoring flip-flop should be in its initial zero position.

Let us consider multiplication. In automatic computers using the binary system, multiplication is usually by direct code. In this case the multiplier controls the addition of the multiplicand to the partial product. The multiplicand is added to the partial product if, after the regular shift to the right of the partial product and multiplier, there is a unit in the next digit place. From the point of view of monitoring, the multiplication of two binary numbers can be treated in the following simplified way. The product is obtained by adding the multiplicand as many times as there are units in the multiplier. From this we derive a simple rule.

3. The number of units in the product plus the number of all the carries during multiplication (in all additions of the multiplicand to the partial product) will be odd only when the number of units in both multiplier and multiplicand is odd.

Let us suppose, for example, that there are no carries in the addition of the multiplicand to the partial product. Then there can be an odd number of units in the product only if there is an odd number of additions (an odd number of units in the multiplier) of a multiplicand with an odd number of units.

From rule 3, it is essential that, when counting the factors, the monitoring flip-flop should be in position 1 only when the number of units is odd in both factors. During the multiplication it counts the carries, and when the product is written it should be in position 0.

Let us now consider some elementary operations which are met with in working with binary codes: number shift, formation of inverse and complementary code, and rounding off.

In shift of numbers (as, for instance, in shifting the partial product to the right in multiplication, when a double number of digit places is not required) there can be a "loss of a unit" in the result, which destroys the zero balance in the monitoring flip-flop in writing the result. Therefore, in shifting binary codes all units exceeding the limits of registers must be registered on the spot by the monitoring flip-flop.

Formation of inverse code is, in effect, the replacement of zeros by units and vice versa. Therefore, if the number of digit places is even, inverting the code does not change the number of ones in the monitoring count; if the number of digits in the code is odd, the number of ones changes. In this case, a one must be added to the monitoring flip-flop.

Complementary code is formed from the inverse code by adding one in the lowest digit place. Obviously this unit and all additions arising from it must be discounted by the monitoring flip-flop. If the unit is added with the addition of two codes, the carries are discounted once. The result of rounding-off is discounted similarly.

In carrying out certain operations, such as multiplying numbers by direct code, the signs are dealt with separately This is usually done according to simple rules. In multiplying, the signs are added in pairs, and so can be discounted by the monitoring flip-flop, which can thus check the digit part of the code together with the sign.

Division in the binary system is a definite series of the operations considered above, and so can, in principle, be checked by the number of units in the codes and in the code of the result. However, simple practical rules like those used for addition and multiplication cannot be formulated. In general, division is comparatively seldom called for in calculations, and if it is necessary it can be checked by a programme, or by means of multiplication.

The monitoring method which has been described checks the working of a serial arithmetic unit fairly completely. A unitary error, or an error changing the number of digits in the code of the result plus the number of carry pulses into an odd number, is immediately detected by the monitoring flip-flop. However, there are some errors which may remain undetected. One such error is the absence of a carry pulse at output V. For this reason, carry pulses should not be applied direct to the monitoring flip-flop

from output V. It is best to insert a unit for detecting a carry by means of a combination of the pulses at inputs I, II, and III. For instance, all the inputs to I, II, and III can be supplied by different delay lines to a supplementary flip-flop, which sends a pulse to the monitoring flip-flop on changing from position 1 to position 0. Before the start of the next working cycle of the adder, the supplementary flip-flop is set in position 0.

We must assume that "absolute checking", which detects every error, is a practical impossibility. However, in some cases it is possible to reduce the probability of letting an error pass. The means of checking the arithmetic unit considered here can well be used, with checking of the writing and reading of codes, with the aid of a checking digit, as considered in Ref. 1 and realized in the Czechoslovak automatic computer (Ref. 2).

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L. N. KOROLEV

METHODS OF SELECTING THE REQUIRED WORD FROM A DICTIONARY

In automatic translation from one language into another, the first necessity is to find a word in the dictionary. If, say, an English word is to be translated, then we have to determine from its code the address of the information concerning it, or the place in the store that holds all the data on this word necessary for the further working of the translation programme. These data include the grammatical characteristic (part of speech, and other attributes) and also the "Russian number", which is the address of the corresponding translation in the Russian part of the dictionary.

The problem of finding the required information can be set out as follows. Let the information about the first word in the English dictionary be held in cell 1, and information about the second word in cell 2, and so on.

In Fig. 1, evenly-spaced points are numbered in order. At each point (i) we construct an ordinate, equal in value to the code i of the English word, where i is its serial number in the dictionary and at the same time the address of the corresponding data.

In this way we obtain a discrete function $y_i = S(i)$, given for several whole numbers. The problem of finding the required word reduces to determining from a given ordinate of the appropriate abscissa the function $y = S(x)$.

There are several methods of solving this problem. The choice of method has a marked effect on the speed of the programme and on the means of storing dictionary

information. The simplest method consists of a comparison of the code of the word to be translated with the code of every other word in the dictionary, beginning with the first. Simultaneously, the number of words tried is counted. This process continues until the codes correspond. In this case the number of words compared is equal to the number of the cell holding the required information.

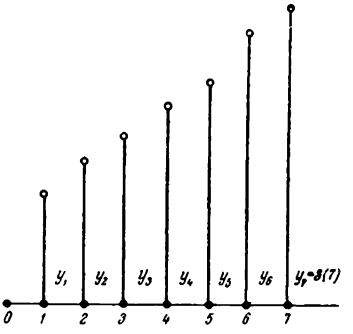

Fig. 1.

The programme realizing this method consists of selection of the code of a word from a dictionary of standard cells (15 to 20 operations) and comparison of the contents of the standard cells with the selected word. Thus finding one word takes an average of $k = a.\frac{1}{2}N$ operations, where a is the number of operations made in selecting the code from the dictionary and in comparing it with the required code, N is the capacity of the dictionary, and $\frac{1}{2}N$ is the average number of trials in looking for one word. When $N = 1000$, $a \approx 20$, $k = 10{,}000$ operations.

With this method we need to hold in the store the codes of the English words in the dictionary and their attributes in sequence of the corresponding codes. This organization of the dictionary makes it fairly simple to supplement it and to introduce alterations.

The second method requires that the codes of the English words should be arranged in alphabetical order. Information about words and their attributes is arranged in the same order. Then, to find a word, it must be sought in a group of codes of words beginning with the same letter or two letters.

Finding the section of the dictionary corresponding to the first letter takes 26 comparisons and 26 transfers of command. At the cost of these 52 operations we can reduce the size of the dictionary in which the word has to be sought by an average of 26 times, and shorten the time by half.

The best method from the point of view of use of machine time, and the simplest in logic, is that called "halving". For this method, the codes of the words in the dictionary must be arranged in a strictly ascending or descending order. The codes are regarded as numbers. With this disposition of the codes, the function $y_i = S(i)$ increases monotonically; that is, for any i,

$$S(i - 1) < S(i) < S(i + 1),$$

and in consequence a method analogous to the "false position" method for finding the root of a monotonic function can be used to find the abscissa for a given ordinate.

The method is as follows. The required word is sought in the middle of the dictionary, by comparing it with the code which has the serial number $\frac{1}{2}N$ (For the sake of simplicity we shall take it that $N = 2^k$). If the code of the required number is greater than this, search must be made in the half of the dictionary from $\frac{1}{2}N + 1$ to N; that is, in the lower half of the dictionary. In the other case, search must be made in the upper half, from 1 to $\frac{1}{2}N - 1$. Search for the word in the selected half is carried out by the same method of halving. Each trial halves the part of the dictionary in which search must be continued. Since the capacity of the dictionary is limited, we need not more than k trials, given by

$$k = E(\log_2 N) + 1,$$

where E shows that we must take the integral part of $\log_2 N$. For instance for N = 1000 words, $k \approx 10$.

It can be arranged that each trial takes not more than 5 or 6 machine operations. With a speed of 10,000 operations a second, finding one word takes about 0.006 sec.

One advantage of the halving method is that increasing the size of the dictionary increases the time of search

only slightly, in proportion to $\log_2 N$. The arrangement of the codes in ascending order is easily accomplished by the machine itself.

There is another possible method of search, which requires for its realization the preliminary determination of a convenient analytical form of the function $i = S^{-1}(y_i)$; that is, the inversion of $y_i = S(i)$. Such an analytical form can in fact be obtained by replacing the discrete function $y_i = S(i)$ by the continuous monotonic function $y = \tilde{S}(x)$, constructed approximately from the y_i ordinates. In this case the search for a word in the dictionary will consist of calculation of the value of x of the function $x = \tilde{S}^{-1}(y)$ for the given code y. The calculated value x (or the whole number nearest to x) will be the address of the information on the word whose code is equal to y. It is obvious that in this case there is no need to hold the codes of the English words in the dictionary. The search for a word (that is, the determination of the address of the information concerning it) is replaced in this case by calculation of the value of a given function.

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N. Ya. MATYUKHIN, O. V. ROSNITSKII

THE ROLE OF THE FERRITE CORE IN A MATRIX STORAGE UNIT

Descriptions have been published of magnetic stores of the matrix type, using toroidal cores made of ferrites with a rectangular hysteresis loop for storage of binary digits 1 and 0, and employing the method of coincidence of current pulses for selection of the required memory cells (Refs. 1, 2, 3).

The following are the basic requirements of these units: 1) reliability of storage of information; 2) reliable discrimination of the reading signals for 0 and 1 against a background of noise from partial excitation; 3) high speed.

We shall consider the amplitude and duration of current pulses in the selector leads of the matrix which are necessary to satisfy these requirements.

Since high speed in a storage unit conflicts to some extent with reliability of storage and discrimination, the suitability of a ferrite core for a matrix of a given high speed must be established after the maximum speed has been determined.

Speed is restricted mainly by the magnetic viscosity of the ferrite cores storing the information, in accordance with the relation (Ref. 4):

$$(H_m - H_0)\tau = S, \qquad (1)$$

where

S is a constant depending on the physical properties of

the material of the core;

τ is the time of flux reversal, measured by the voltage in the output winding at a level 0.1 of the amplitude value;

H_0 is the critical field, with which begins the non-reversible displacement through 180° of the boundaries between the domains;

H_m is the applied flux-reversing field.

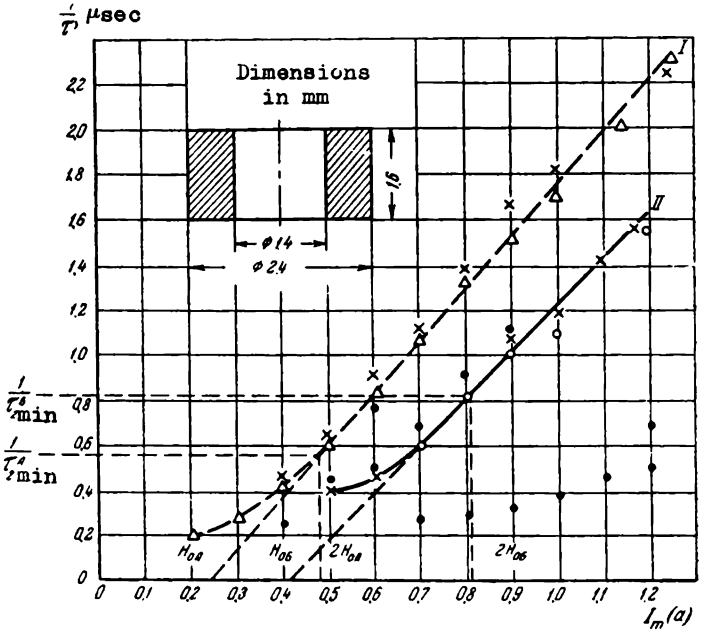

Fig. 1. Dependence of flux reversal time on amplitude of flux reversing current.
I core type A II core type B

In measuring the time of flux reversal, we use square current pulses with a front lasting a much shorter time than the time of flux reversal.

Fig. 1 shows experimental graphs for ferrite cores of

Soviet manufacture, all of the same dimensions, but differing in their hysteresis properties. It is evident that equation (1) holds for high values of the flux-reversing field (work on a restricted loop), and that the value of H_0 is determined by extrapolation of equation (1) to the point $H = H_0$, $\tau = \infty$.

So that the partial excitation field affecting cores on the selected leads should not cause a considerable development of non-reversible processes in the cores, it must not exceed the value H_0. If, in this case, the flux reversing field affecting the selected core raises the partial excitation field by k times, the maximum admissible value for the flux reversal field is

$$H_m = kH_0. \tag{2}$$

The minimum time of flux reversal of a core in a matrix is defined from (1) and (2)

$$\tau_{k\,\min} = \frac{S}{(k-1)H_0}. \tag{3}$$

Fig. 1 gives the minimum values for the time of flux reversal for both types of core when they are used in a matrix with coincidence of two currents ($\tau_{2\,\min}$). Since, for materials with a sufficiently square hysteresis loop, the value of the critical field H_0 is close to the value of the coercive force H_C, equations (1), (2), and (3) can be rewritten in the form

$$(H_m - H_C)\tau = S, \tag{4}$$

$$H_m = kH_C, \tag{5}$$

$$\tau_{k\min} = \frac{S}{(k-1)H_C} \cdot F \tag{6}$$

The maximum value of the frequency of reversal $F_{k\,\max}$ for a store in which coincidence of currents is used for both reading and regeneration can be determined as follows. To establish a reading-regeneration cycle it is necessary to apply to the matrix at least two current pulses (a reading and a regeneration pulse); that is, the duration T of this cycle is always greater than twice the value of the duration of a current pulse τ_p. As for

the value of τ_p, it must be somewhat greater than the corresponding time of flux reversal $\tau_{2\,min}$, measured by means of current pulses with very steep fronts. Current pulses of this kind present considerable difficulties in an actual storage unit. Taking $\tau_i = 1.5\ \tau_{k\,min}$, and $T = 2.5\ \tau_p$, and bearing equation (6) in mind, we get

$$F_{k\,max} \approx \frac{k-1}{4S} H_C. \tag{7}$$

The value of S determined from Fig. 1 is approximately equal to 1 oersted per μ sec, which corresponds to the values given in the references for magnesium-manganese ferrites (Ref. 5). So by using similar materials in the storage unit we can obtain the maximum operational frequency:

$$F_{k\,max}(\text{Mc/s}) \approx \frac{k-1}{4} H_C \text{ oersted} \tag{8}$$

If the matrix works by coincidence of two currents ($k = 2$), then:

$$F_{2max}(\text{Mc/s}) \approx 0{,}25 H_C \text{ oersted} \tag{9}$$

In consequence of the departure of the hysteresis loop from the square form, working at maximum speed gives, with partial excitation, a considerable variation of remanent induction, and a small signal-to-noise ratio.

Fig. 2 shows the voltage waveforms in the output winding of a type A core with its state varying in accordance with the corresponding sections of the hysteresis loop, taken in operating conditions close to the maximum speed in a matrix with coincidence of two currents. A unit reading signal voltage is induced if the core changes its state along the path $0q1(u_c)$ or $1'p0(u'_c)$. In the second case, u'_c is a unit reading signal from a core subjected to half-excitation. A half-excitation noise voltage (u_n) is induced in the case of movement along the path $1p'1'$. From these diagrams we can see that at maximum speed the change of remanence in a core of type A is about 50% of the initial value. The ratio of the reading signal of unity to the noise of half-excitation varies with time. The reading gates, through which the read-out information is sent from the store, must be opened by a

short pulse at the time when this ratio has its highest value. At maximum speed, the ratio is about 10 for ferrite A.

Similar results are obtained for ferrite B. Variation of remanence with half-excitation is about 30%, and the highest signal-to-noise ratio is 15.

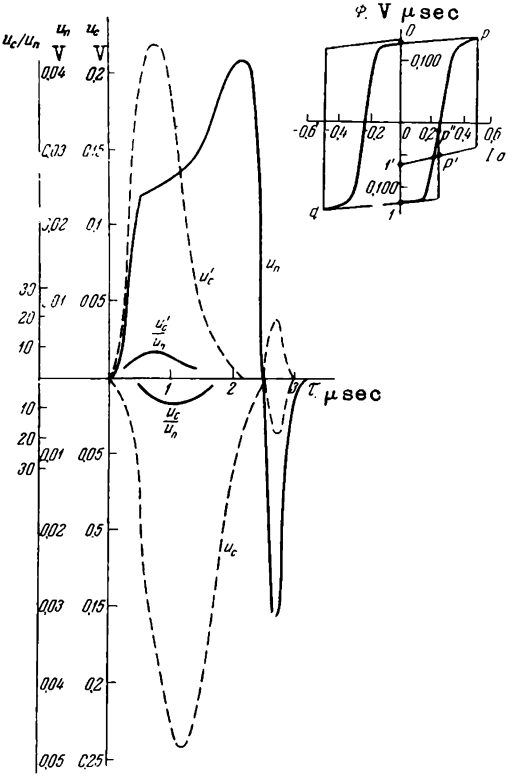

Fig. 2. Voltage waveforms in the secondary winding of a core of type A (I_m = 500mA).

We should observe that, as a result of the restricted duration of a current pulse, the state of the core with half-excitation does not change as far as point p'' in

Fig. 2, but only as far as point p', as the half-excitation field exceeds the threshold field essential for vigorous development of non-reversible processes only by a little, and the time of flux reversal grows steeply. Thus with a single half-excitation the magnetic viscosity creates an apparent increase of squareness. However, repeated half-excitations will demagnetize the core.

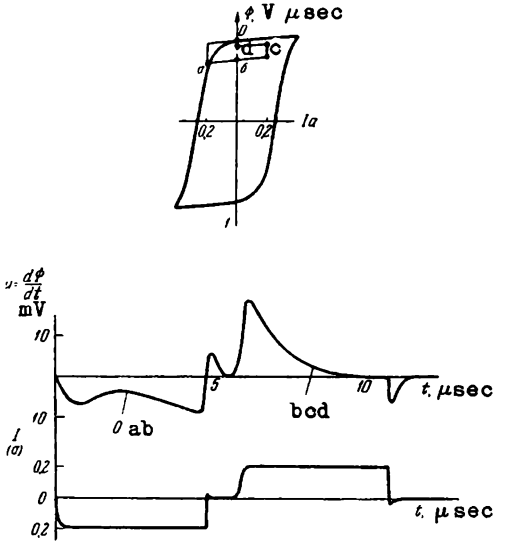

Fig. 3. Influence of the prevailing magnetization on speed of flux reversal.

Operation at maximum speed is undesirable from the point of view of reliability of the store. The noise and the non-reversible change of flux with half-excitation are considerable; and there is great instability even with small current variations, since with half-excitation the core changes its state along the steep section of the hysteresis loop.

Let us now consider in greater detail the operational reliability of a matrix storage unit. One of the causes of unreliability is erasure of information by repeated half-excitations. A second cause is growth of the total noise in consequence of the accumulation of noise from half-excited cores in the common reading winding.

Although the process of demagnetization of ferromagnetic materials by a series of current pulses has not been sufficiently studied, we can mention here some basic factors influencing the demagnetization of a core.

In materials with a square hysteresis loop, with small enough fields the speed of flux reversal (for non-reversible processes) depends on whether or not the direction of the magnetizing force is the same as the direction of the prevailing magnetization of the core.

Fig. 3 shows waveforms of the excitation of a core which is near saturation point. The speed of flux reversal is several times less when the magnetizing force opposes the field of the remanent induction than when it is in the opposite direction. Also, to return a core to its initial state (or one sufficiently near to it) the second pulse can be smaller, both in length and amplitude, than the first.

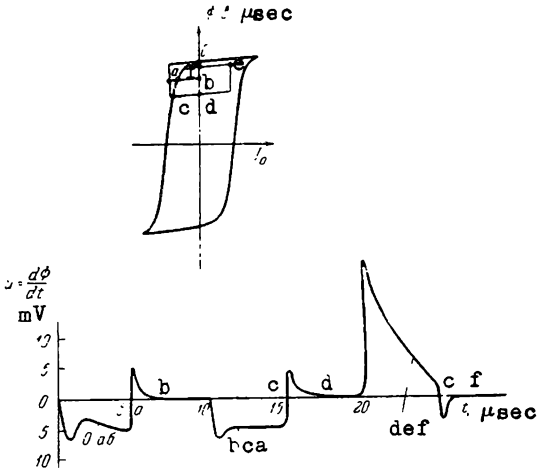

Fig. 4. Influence of direction of prevailing magnetization on speed of flux reversal.

Fig. 4 shows waveforms of the recording of zero, when the core is subjected to the consecutive action of two demagnetizing pulses. We see that, with proper selection

of the value of the current, a pulse affecting the core in the direction of the prevailing magnetization returns it almost completely to its initial state after a double half-excitation in the opposite direction. This phenomeno counteracts the demagnetization of a saturated core when it is excited by a succession of current pulses of changing sign.

With increase of the amplitude of demagnetizing pulses, however, this property of the magnetized core can no longer compensate completely for the development of non-reversible processes, as a result of which demagnetization and, therefore, erasure of information, take place.

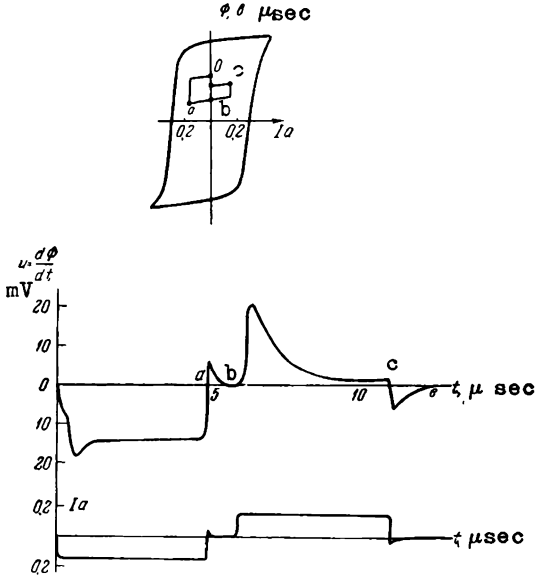

Fig. 5. Influence of intensity of prevailing magnetization on speed of reversal of flux.

In this case we should also bear in mind that the manifestation of these properties of the magnetized core decreases with departure of the core from its saturated

state. Figs. 3 and 5 show oscillograms illustrating this phenomenon.

To determine the minimum amplitude of the erasing pulses I_{erase}, the core was demagnetized by a sufficiently long sequence of pulses of the same polarity to the state $B_{rem} = 0$. The results of measurements for different working cycles of flux reversal are shown in Fig. 6. The choice of the working cycle is determined by the value of I_m. Curves for the demagnetizing current I_{erase} and for

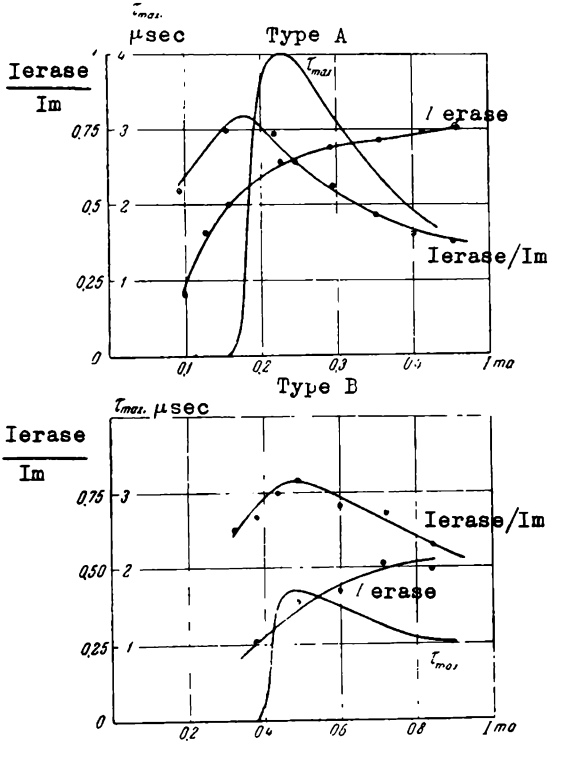

Fig. 6.

the ratio I_{erase}/I_m are given as functions of I_m. The

introduction of compensating pulses of opposite polarity, which is often done in practice, slightly increases the value of the minimum demagnetizing current, for the reasons given above.

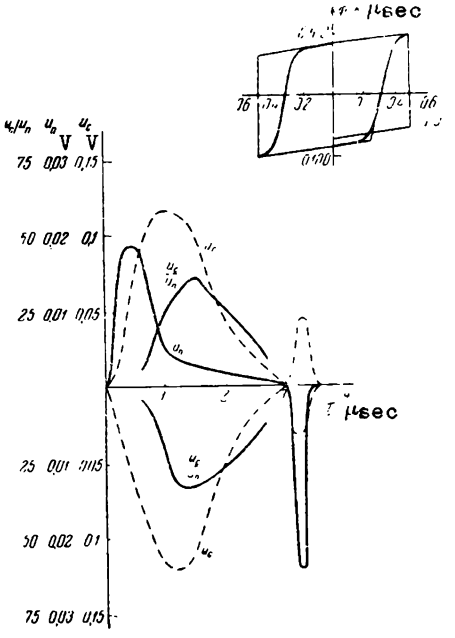

Fig. 7.4 Voltage waveforms in the output winding of a type B core with optimum operating conditions (I_m = 500 mA).

In a matrix using coincidence of two currents, to avoid erasure the quantity I_{erase}/I_m must in all cases be greater than half. At the same time we must bear in mind that when I_{erase}/I_m is slightly more than half, a considerable decreas in the value of the reluctance in the core, and a considerable fall in the magnitude of the useful signal, take place The maximum of the ratio I_{erase}/I_m, which determines the most reliable working regime of the matrix from the point

of view of erasure, corresponds to those values of I_m which create fields near in magnitude to the critical field H_0 (see Fig. 1).

Voltage waveforms in the output winding of a type B core in such a regime are shown in Fig. 7. It is interesting to note that for these currents the signal-to-noise ratio is greatest both in area and amplitude at the most advantageous moment, characterized to a known degree by the value of τ_{max} in Fig. 6, which determines the shift of the maximum of a unit reading pulse with reference to the front of a current pulse.

Thus for avoidance of erasure, and also for the best signal-to-noise ratio in one core, the most reliable high speed working is at about half the maximum (in Fig. 1, when $H_m = H_0$). That is, when, from equations (7) and (9),

$$F_{k\,opt} \approx \frac{k-1}{8S} H_C, \tag{10}$$

$$F_{2\,opt\,(Mc/s)} \approx 0.12 H_C \text{ oersted} \tag{11}$$

Expressions (10) and (11) permit us to evaluate the high speed of a matrix type store with ferrite cores. In particular, for the samples we have investigated the operational frequency in a matrix with coincidence of two currents is about 60 kc/s (ferrite A) and 120 kc/s (ferrite B). Besides this, it follows from (10) that a simple decrease of the coercive force of the materials without corresponding diminution of secondary action in them (decrease of S) can only lead to decrease of speed or to complication of the commutation circuits (increase of k) in order to achieve the same high speed.

In conclusion, let us consider the question of the noise resulting from double coincidence in a matrix unit.

To minimize the effect of noise, the reading winding is threaded through the cores in such a way that half-excitation signals of two cores oppose one another, and so are compensated to a known degree. However, compensation is incomplete, even with absolutely identical cores, chiefly because the half-excitation signals have different values depending on the magnetization of the core.

The difference in magnitude and shape of the half-excitation signals is advantageous when the magnitude of a current is sufficient to develop non-reversible flux reversal processes. The influence of two factors is then felt: a kind of magnetic anisotropy (or quasi-elasticity) of the magnetic material, already mentioned (see Fig. 3), and the secondary effect of the previous magnetization.

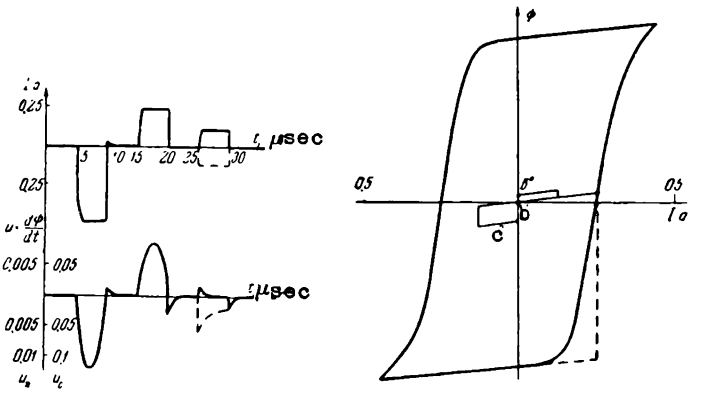

Fig. 8. Influence of secondary effect on speed of flux reversal.

If anisotropic properties are determined by the value of the remanent induction, the secondary effect depends on the path by which the core attains the given state. Fig. 8 shows oscillograms of two cases of flux reversal of a core with the same initial state, attained by two different paths. To obviate the influence of magnetic anisotropy of a magnetized core, the demagnetized state ($B_{rem} = 0$) was chosen as the initial state. It is clear that the speed of flux reversal lessens if a pulse bringing the core into the initial state coincides in direction with a pulse reversing the flux.

Fig. 9 shows oscillograms of stable noise with half-excitation of cores holding either 0 or 1, and the difference between these disturbances.

In the worst possible case, the cores marked + in Fig. 10 hold 0, and those marked – hold 1, or vice versa.

The noise is then equal (in a large enough matrix) to the difference between the signals (see Fig. 9) multiplied by the number of cores in a line.

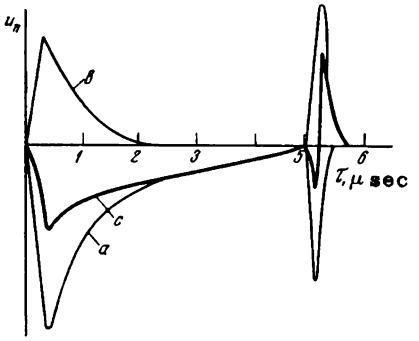

Fig. 9. Oscillograms of disturbances with half-excitation of cores containing code 0 (a), 1 (b), and the difference between the two disturbances (c).

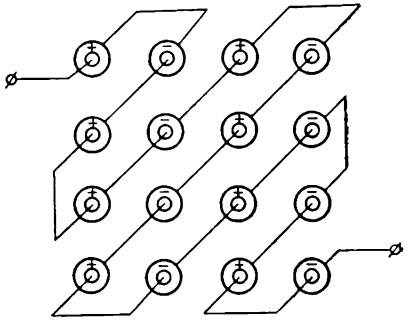

Fig. 10. Circuit for compensation of noise in the reading winding.

It is obvious that the operating conditions of the cores must be selected in such a way that the difference between the disturbances is as small as possible. In practice this is carried out when the value of the flux reversing field is near to the optimal regime (in our case, to H_0).

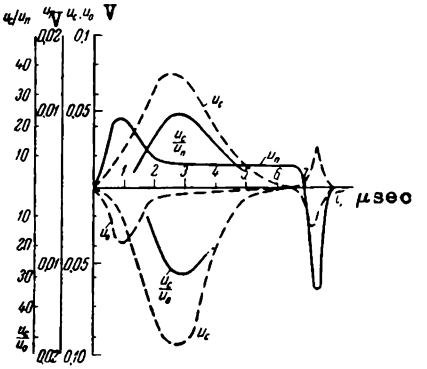

Fig. 11. Voltage waveforms in the output winding of a type A core in reading out 1 (u_c, u'_c) and 0 (u_0); I_m = 300 mA.

Finally, the ratio of a unit reading signal to a zero reading signal in a single core during one gating interval is in practice so large that it cannot cause any apprehension in the designing of a storage unit. This is clear from Fig. 11, which shows a zero reading signal from a core subjected to half-excitation, and reading signals for unity.

The above discussion of the suitability of ferrite cores for use in a matrix store does not refer to certain specific properties of ferrites. For instance, their low Curie point means that the reliability of the store depends to a great extent on temperature. However, the methods of appraisal which have been described permit the selection of a range of pulse amplitudes and durations with which we can hope to obtain reliable working, and of which more detailed investigations should be made.

The measurements on which this paper is based were carried out in the Laboratory for Control Machines and Control Systems of the Academy of Sciences of the U.S.S.R. R.P. Shidlovskii, engineer, and V.M. Mineev, technician, helped take the measurements. The cores were prepared according to the technique developed by A.A. Kosarev and his co-workers, from the powders K-65 (ferrite A) and K-28 (ferrite B).

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Yu. N. GLUKHOV, O. V. ROSNITSKII

RELIABILITY OF A MATRIX TYPE MAGNETIC STORE WITH LINEAR SELECTION

Magnetic stores of the matrix type, working on the principle of coincidence of currents and storing information in ferrite cores with a square hysteresis loop, are widely used at the present time. In these devices coincidence of currents can be used for reading as well as for writing information. When it is used for reading, there arises the problem of separating the reading signal from the background of noise from partial excitation. If coincidence of currents is not used for reading, partial excitation of the cores in reading does not arise; that is, there is no partial excitation noise. In some instances (with a store of small capacity, or if matrix commutators are used) a scheme of this kind, which we shall call a matrix with linear selection, is justified, as it can increase reliability and speed.

The present paper discusses operational tests of cores in a matrix with linear selection of 16 digit places, using cores of K-65 material with external diameter 2.4 mm, internal diameter 1.4 mm, and thickness 1.6 mm.

Fig. 1 is the block diagram of the store. Coincidence of two currents is used here only for writing and regenerating scanned information, and reading is achieved by sending a full flux-reversing pulse to the selected address bus, so that there is no half-excitation noise. In writing as well as in reading a pair of current pulses is sent to the selected address bus (Fig. 2).

The first pulse, of amplitude 2I, sets all the cores of the selected bus at position 0; that is, it produces

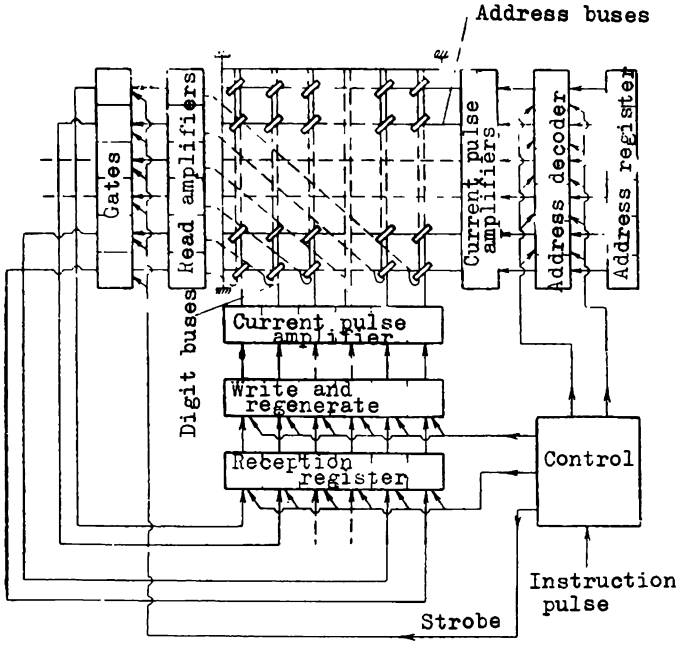

Fig. 1. Block diagram of matrix store with linear selection.

reading of the number. If a reading operation is carried out, the second pulse I serves for the regeneration of the scanned information, by coincidence of this pulse with similar pulses sent to those digit place buses where 1 was read out. If a writing operation is carried out, the second pulse in the same way permits the writing of 1 in those digit places in which it should be written. If 0 is written, no current pulse is sent to the digit place.

For a reading cycle, a start pulse (reading instruction) is supplied to the control block, after which the block gives out a series of pulses, as shown in Fig. 3a. A pulse clearing the receiving register sets all its flip-flops at 0. At the same instant as the reading pulse, a strobe pulse is sent to the gates of the reading channel, permitting the information to be sent to the reception

register. Rewriting is effected from this register when the next pulse occurs.

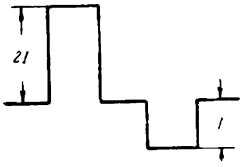

Fig. 2. Current pulses in address busbars.

For a writing cycle, a writing instruction pulse is supplied to the control block. The information to be

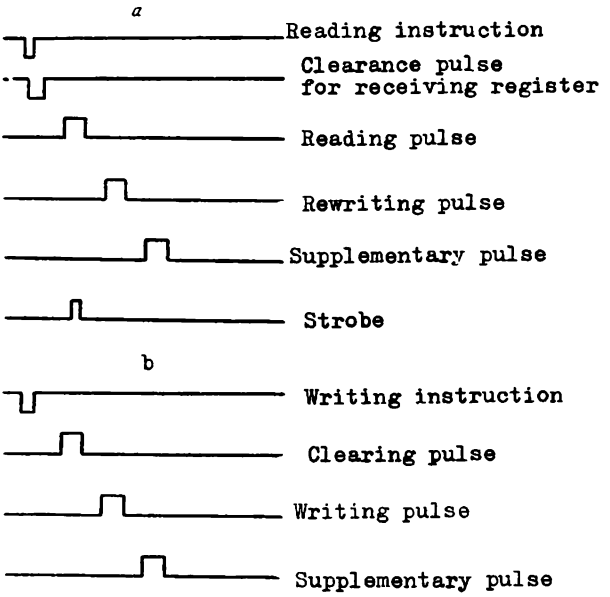

Fig. 3. Sequence of pulses sent from the control block during the operations of reading (a) and writing (b).

written is set up in the receiving register. The control block sends out a series of pulses at intervals as shown in Fig. 3b. A reading (clearing) pulse sets all the cores of the address in which the information is to be written in position 0.

A supplementary pulse brings about bi-polar half-excitation in the digit buses, which affects the reliability of storage of information. Let 0 be written in a digit

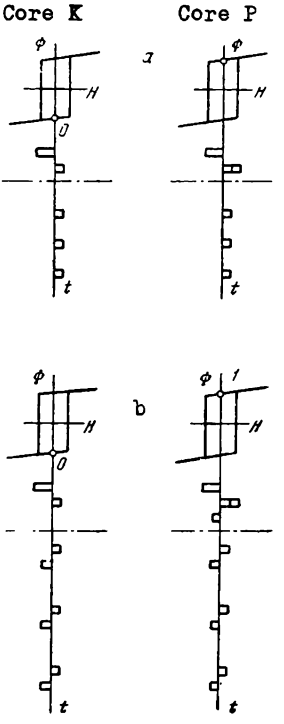

Fig. 4. Effect of current pulses on a core when 1 or 0 is written, with consequent half-excitation.
a) unipolar half-excitation
b) bi-polar half-excitation.

place core K and 1 in digit place core P of one address

(see Fig. 4). These cores can be energized an indefinite number of times by half-excitation currents when 1 is written or regenerated in the same digit places in other addresses.

With unipolar half-excitation, this can lead to decrease of remanent induction in cores holding 0; it can "erase" 0 (Fig. 4a). It is obvious that the process of "erasure" will be different if the core is half-excited by bi-polar pulses of the same amplitude. In this case 0 and 1 are subject to "erasure" (see Fig. 4b).

The currents in the buses of the matrix have a square form with fronts of the order of 0.2 - 0.3 μsec. To stabilize these currents, resistors are connected to the buses of the matrix. As the number of flux-reversed cores in an address can vary, resistors chosen so that they ensure constant current with change of load are connected to the buses of the addresses. In the experimental matrix used in the investigation, 10 Ω resistors were connected to the digit buses, and 25 Ω resistors to the address buses. These resistors also provide a means for measuring currents.

In the output winding of the matrix, which serves each digit place, there occurs a voltage pulse which coincides with the reading pulse. Its amplitude and duration depend on what was written in the given digit place. A reading signal 1 triggers the corresponding flip-flop of the register into position 1; a reading signal 0 cannot change the position of a flip-flop. Discrimination between reading signals 1 and 0, each of which changes in its own fashion with variation of the magnitude and duration of current pulses, is made by adjustment of the bias on the control grid of each gating valve individually.

To investigate the reliability of storage in the absence of erasure, the specific amplitudes and durations of the currents in the matrix were established. The timing of the strobe, and the grid bias of the gating valves of each digit place were selected so that: a reading signal 1 from a core not subjected to half-excitation should be sufficiently great at the output to trigger the flip-flop of the register; and a reading signal 0 at the valve output should be zero.

An arbitrarily-chosen number was set by hand in the register of the first address. This address was then subjected to half-excitation by uninterrupted reading and

regeneration of units in all digit places of a second address. After half-excitations numbering several tens of thousands, the control block was disconnected, the register was set in position 0, and transition to reading and regeneration of the number previously written in the first address was achieved by hand. If, when the control block is connected, the previously written information is set in the reception register, this means that the operating currents selected do secure non-erasible storage.

In this way the regions of non-erasible storage were established for specific fixed positions of the strobe and bias values of the reading valves (see Fig. 5) under the action of single-pole and bi-polar half-excitation.

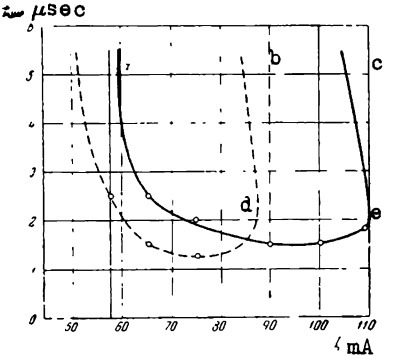

Fig. 5. Boundaries of reliable operation of a matrix for:
a) bi-polar excitation (——)
b) single-pole excitation (- - -).

Of course, with other bias values and other positions of the strobe, other regions than those shown in Fig. 5 result; that is, these regions do not include the whole range of currents with which it is possible to achieve non-erasible storage.

We should observe that in stores of large capacity with planar selection, where reading is carried out by coincidence of currents, reliability depends to a high degree on the ratio of the reading signal to the half-excitation noise. For this reason, achieving non-erasible storage in a matrix with linear selection for several current

values does not yet imply the possibility of reliable operation of a store of large capacity with planar selection for these same currents.

Figs. 7 to 9 show the voltage waveforms in the output winding of a core, taken within the region of currents in question. They were observed when the core was subjected to different series of current pulses (Fig. 6).* The

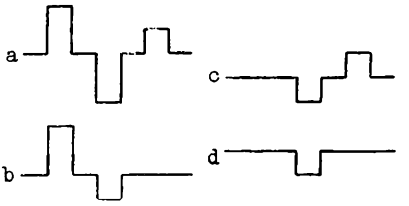

Fig. 6. Sequences of current pulses which can excite any core in the matrix.

series of current pulses c half-excite a core previously subjected to either series a or series b. The one-polar half-excitation (series d) affects a core previously excited by series b. These waveforms make it possible to study the reading signals 1 and 0, the first and the stable disturbances; this enables us to obtain some idea of the possibility of employing these or other regimes in a store with planar selection.

For regions of current with small amplitude and duration of pulses (lines ab and cd in Fig. 5) a small difference between reading signals and an appreciable difference between the first and stable disturbances is characteristic.

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*Voltage pulses in the reading winding arising with action of one of these sequences are correspondingly denoted by a,b,c,d. For convenience of comparison of reading signals 1 and 0, voltage pulses corresponding to the sequences of current pulses a and b are shown together; voltage pulses corresponding to series b are shown by the dotted line, without blips due to the trailing edge. Voltage pulses corresponding to series c and d are shown for the case when these series are applied to a core previously excited by series a, unless otherwise indicated.

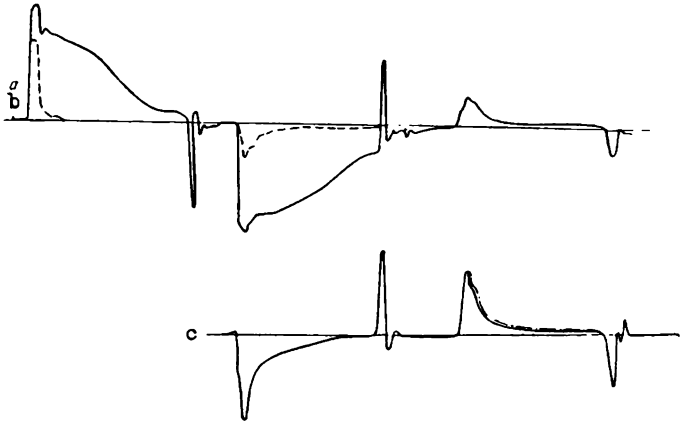

Fig. 7. Voltage pulses in reading winding ($I_{half\text{-}excit.}$ = 100 mA; duration of current pulses 5 μsec).

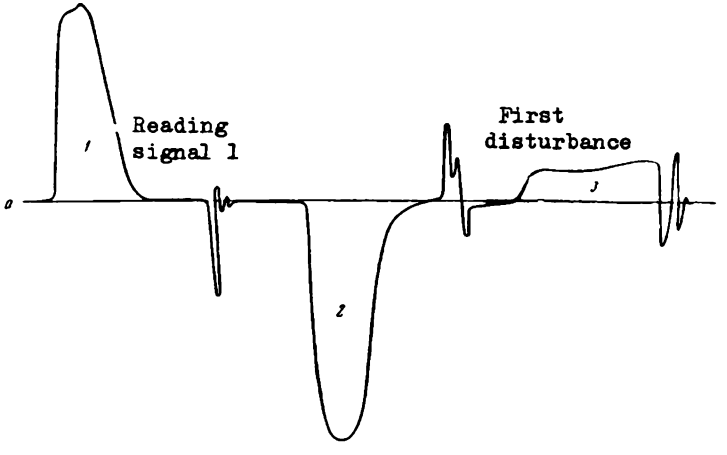

Fig. 8. Voltage pulses in output winding of a core (counter-magnetization current about 400 mA).

The use of these regimes in a matrix store with planar selection may be impossible, since incomplete compensation

of disturbances in the common reading winding of each plane of the matrix makes the reading signal 1 indistinguishable from 0 on the background of noise.

Fig. 9. Stable noise in a core holding unity during action of half-excitation currents of 200 mA.

A sufficiently high ratio between the reading signals 1 and 0, and a small noise difference, make it possible to use planar selection matrices with currents of about 100 mA and duration of about 5 μsecs (Fig. 7).

The use of large currents is impossible even in a matrix with linear selection. As the experiments showed, nonerasible storage is not secured if the current exceeds 150 mA.

This is confirmed by study of the waveforms taken in these regimes. Let us consider Fig. 8. A full countermagnetizing current pulse of 400 mA with 5 μsec duration reverses the flux of a core along the determined hysteresis loop. As a result the induction in the core is changed to the magnitude $2B_0$. The area of the voltage pulse 2 (Fig. 8), is proportional to this change of induction. The first current pulse of half-excitation provokes a change of induction by the magnitude $B_0/2$, since the area of the first disturbance constitutes about a quarter of the area of the voltage pulse corresponding to full flux reversal of the core.

Increase of the area of the subsequent disturbances is probably caused as follows: the second half-exciting current pulse, having polarity opposite to the first, does not fully compensate for the loss of induction from the first half-excitation (see Fig. 10), and the subsequent

half-exciting pairs of current pulses cause the development of a non-reversible process in the core.

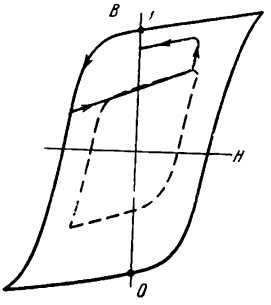

Fig. 10. Change of induction caused by the first two half-excitations after writing 1.

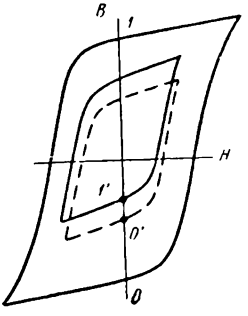

Fig. 11. Stable partial cycles for half-excitation currents after writing 1 (——) or 0 (- - -).

If the voltage pulses (Fig. 9) were identical in form and amplitude, we might suppose that flux reversal in a

core by half-excitation current pulses in a stable regime takes place along the symmetrical partial cycle shown by the dotted line in Fig. 10. However, the form of these pulses permits us to suppose that change of induction in the core takes place along an asymmetrical partial cycle (see Fig. 11). Thus the effect of the half-excitation current pulses on a core previously magnetized to the value + B_0 (writing of 1) leads to a decrease of the remanent induction; that is, to partial erasure of 1.

Now let this same core be excited again by pulses of the sequence shown in Fig. 6b, and then by half-exciting bi-polar current pulses (Fig. 12). In this case we must

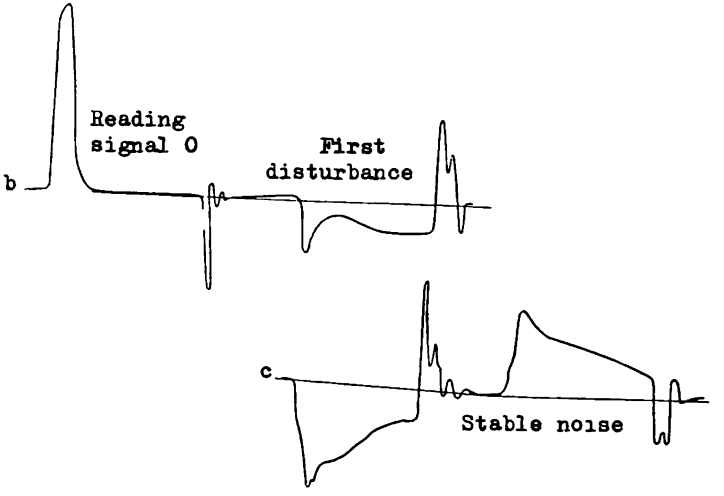

Fig. 12. Voltage waveforms in winding of core with half-excitation pulses of 200 mA amplitude and 5 μsec duration, after writing 0.

bear in mind that after the core is demagnetized to the value $-B_0$, it is subjected anew to two half-exciting pulses of one polarity, then to half-excitations of changing sign. The conjectural state of the stable partial cycle for this case is shown by the dotted line in Fig. 11. Thus, after the action of a large number of half-excitations on a core previously magnetized to a remanence value of $-B_0$, this core is magnetized to the value $-B_0/2$.

Almost the same value of induction is obtained after a great number of half-excitations of a core previously magnetized to the value + B_0 (see Fig. 10).

Thus, as a result of the effect of half-excitations, the difference between the reading signals 0 and 1 becomes so small that it is in practice impossible to distinguish between them.

The work* we have carried out has shown the possibility of obtaining non-erasing storage in a matrix of ferrite cores of U.S.S.R. manufacture working with square current pulses of duration 2 to 5 μsec with half-excitation currents of 60 to 120 mA. In this case the best signal-to-noise ratio is obtained with currents of the order of 100 mA with a duration of 5 μsecs. When a matrix with linear selection is used, reliable working is possible with currents highly unstable in amplitude ($\pm$ 30%) and duration ($\pm$ 50%). The presence of one-polar half-excitations leads to a certain amount of contraction of the region of non-erasing storage, the permissible spread of amplitudes being $\pm$ 20%.

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*The work was carried out in the Laboratory for Control Machines and Control Systems of the Academy of Sciences of the U.S.S.R. N.Ya. Matyukhin gave the authors great help in carrying out the work. R.P. Shidlovskii and V.I. Berkutov took part in the construction of the storage device and in the experiments.

E. I. MAMONOV

BASIC NOMENCLATURE AND DEFINITIONS IN AUTOMATIC DIGITAL COMPUTER ENGINEERING*

There is no agreed system of nomenclature in use in Soviet electronic digital computer engineering, despite the fact that a considerable time has elapsed since computers were first developed. The absence of a generally accepted terminology is often the cause of confusion and misunderstanding.

The existing nomenclature of installations, circuits, and concepts in this field has been established quite fortuitously, and does not correspond to the principles of rational terminology. In choosing a standard nomenclature we should be guided by the following main requirements.

1) The most exact and clear expression possible of the nature of phenomena, processes, and operations.

2) Brevity.

3) The closest possible approximation of special technical terms to ordinary speech in order to avoid jargon. This facilitates understanding, and accords with teaching practice.

4) Prevention of confusion with terms from allied fields of science and technology (for instance, electrical engineering and radio engineering) in which these terms are established and have a wide circulation.

5) Avoidance of terms with several meanings.

Let us consider some examples. One of the most

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*Submitted for discussion

important stages in calculation is the storing of digital information, which is often called "pamyat'" (memory), "zapominanie" (memory), "nakopitel'" (accumulator), "fiksatsiya" (fixation) etc. "Memory" reflects a biological concept, and is associated with the phases of generalization of phenomena of the external world and the processes of abstract thought. No machine has such qualities; it cannot "think" or "learn by itself", and so cannot be thought of as a brain.

Electronic digital computers are a new and highly effective means for the mechanization and automation of work. Simple arithmetical or logical operations constituting a process of calculation or of the translation of languages are carried out according to a programme preset by a human operator. The programme consists of instruction codes, which switch the circuits in the required order. It is quite clear that no reasoning processes take place in the machine. What happens is not "remembering", but the storing of the necessary steps of automatic recording and reading of digital information. The words "accumulator" and "fixation" do not express the chief purpose of installations for the storage of information. Also, the word "accumulator" is often used for a summator of the accumulating type. Thus the term "khranenie" (store) is recommended.

Of the three equivalent terms "komanda", "prikaz" (order), and "instruktsiya", the most usual and most widely employed in Soviet writing is "komanda". In foreign practice the word "instruction" is used to designate commands or orders introduced into a machine. Of these terms, the choice should obviously fall on the word "komanda".

By "kod" (code) and "shifr" (chiffre, cypher) we designate the system of symbols used in the presentation of information in the machine. In our literature the word "code" has been the more widely used. It does not conflict with the widely known use of "code" in telegraphy. For this reason we prefer it to the word "cypher".

Logical switching elements are very important and much used in modern machines. They are referred to by the terms "ventil'" (valve), "klapan" (valve, vent), "razreshchayushchaya skhema" (permissive system), "klyuch" (key), and others.

The word "ventil'" (valve) is a term in electrical engineering, used particularly of power-supply rectifier

circuits, and indicates an element which conducts one way only, whereas in computer engineering the term is used in quite another sense. The expression "permissive system" is in fact the contrary of logical restrictive circuits, and so does not include the whole class of logical circuits. Of the terms "klapan" (valve, vent) and "klyuch" (key), we consider "key" to be the more suitable, considering the chief purpose of logical systems; namely, the switching of circuits in accordance with combinations of input signals. The addition of an indication of which kind of "key" (AND, OR, etc.) permits the inclusion of the necessary range of concrete varieties of key circuits.

To achieve brevity without loss of clarity, we admit the convenience of using, besides the expressions "ustroistvo avtomaticheskogo upravleniya" (automatic control unit), "ustroistvo khraneniya" (storage unit), "ustroistvo vvoda" (input unit), "ustroistvo vyvoda" (output unit) etc., the corresponding shorter terms "avtomaticheskoe upravlenie" (automatic control), "khranenie" (store), "vvod" (input), "vyvod" (output), etc.

In the hope of obtaining wider discussion, we propose below a basic nomenclature, with definitions, for high-speed digital computer engineering. Such terms as "zaderzhka" (delay), "liniya zaderzhki ultrazvukovaya, elektromagnitnaya, magnitostriktsionnaya" (ultrasonic, electromagnetic, magnetostrictive delay line) borrowed by computer engineering from allied fields of science and engineering do not change their meanings. A whole set of terms, such as "perfolenta" (punched tape), "perfokarta" (punched card), etc., was established long before the appearance of electronic machines, and do not give rise to ambiguities. Such terms are not considered in this article.*

Avtomaticheskii perevod (Machine translation). Translation of texts from one language into another by means of automatic digital machines.

Avtomaticheskaya tsifrovaya vychislitel'naya mashina (Automatic digital computer). A machine in which arithmetical, logical, and other operations are carried out automatically in accordance with a prearranged programme,

*In preparing this article, consideration has been given to the valuable observations of E.A. Volkov, G.K. Rakov and V.I. Shestakov.

and the information on which these operations are carried out is presented in the form of a discrete digital code.

Adres (Address). Number of the cell in the information store in which information is to be recorded, or from which it is to be taken. Represented as a number code.

Otnositel'nii adres komandy (Relative address of an instruction). An address of an instruction which is obtained by adding the number from the instruction counter to an address for the instruction which is selected from the operational store (usually in one-address machines).

Arifmeticheskie deistviya (Arithmetical operations). The basic operations of arithmetic: addition, subtraction, multiplication, and division.

Arifmeticheskoe ustroistvo (AU) (Arithmetic unit). The part of a digital computer by means of which arithmetical and logical operations on number and instruction codes are carried out.

Parallel'noe (AU) (Parallel arithmetic unit): one in which operations on numbers are carried out simultaneously in all digit places.

Posledovatel'noe (AU) (Serial arithmetic unit): one in which, in contradistinction to the parallel unit, operations are carried out successively, digit by digit.

Bezuslovnyi perekhod (Unconditional transfer). Instruction for automatic transfer to another instruction, the first in number (address) in a new sequence of the programme.

Blokirovka normalizatsii (Blocking of normalization). The automatic suppression of normalization, particularly used in conversion of instructions and to increase speed of addition and subtraction.

Vvod (Input). 1) The equipment used to introduce information into a machine. 2) The operation of introducing information into a machine.

Vosstanovlenie (Regeneration). Compensation of undesirable changes of the codes of information stored in the form of charges on the screen of a cathode-ray tube. It is carried out by re-recording the charges (in tubes with external regeneration) or by a delaying irradiation by a supplementary internal stream of slow electrons (in tubes with internal regeneration).

It is used also in storage units of ferrites, piezoelectric units, and diode capacitor units.

Vremya ozhidaniya (Storage cycle time). Time taken to complete the operation of recording or reading information in the storage unit, starting from the arrival of the signals controlling these operations.

Vyvod (Output). 1) The equipment used in giving out information from a machine. 2) The operation of giving out information from a machine.

Gashenie (Clearance). Setting of the counting and other circuits assigned for storage and transfer of information to zero.

Glavnye impulsy (Control pulses). Signals from the main generator, securing synchronized control of all parts and circuits of a machine.

Gruppa kodov (Code block). A determinate complex of codes of numbers or instructions, considered as a whole.

Gruppovye operatsii (Group operations). These are specified by special instructions, permitting the repetition of groups of identical operations.

Dvoichnaya sistema (Binary system). The system of calculation with a radix of 2, using the symbols 0 and 1, represented in digital machines as two stable states of various physical phenomena or media.

Dvoichnyi razryad (Binary digit place). The number of the place occupied by a binary digit in a binary number or in an instruction. In digital machines there is always a limited number of digit places (see Razryad) limiting the size of the quantities represented in the machine.

Dvoichnaya tsifra (Binary digit). A single symbol, 0 or 1, used to represent numbers in the binary system.

Dvoichnoe chislo (Binary number). A group of binary symbols, composed according to the laws of the binary system.

Dvoichnaya yacheika (Binary cell). An element in digital machines which can have one of two stable states (flip-flop, dynamic binary cell, dynamic trigger, etc.).

Dvoichno-desyatichnoe predstavlenie chisel (Binary-decimal representation of numbers). System of represent-

ation of a decimal number in which each decimal digit is coded in the form of a binary number. For instance, the decimal number 257 is represented in the binary-decimal form as 0010 0101 0111.

Dvoichno-desyatichnoe i desyatichno-dvoichnoe preobrazovaniya (Binary-decimal and decimal-binary conversion). Translation of numbers from the binary system to the decimal system and vice versa.

Deshifrator operatsii (Operations decoder). A part of the automatic control unit by which the codes of operations are converted into sequences of control signals, which are transmitted to other parts of the machine for the automatic accomplishment of these operations.

Dlitel'nost' koda (Code duration). Time necessary for transmitting the code of a number serially, digit by digit.

Dlitel'nost' operatsii (Duration of operation). The time in the course of which an arithmetical, logical, or other operation is completed, including the time of return to store.

Dopolnenie (Complement). A number whose addition to a given number gives as a result in each digit place the radix r. It is obtained by replacing the digits of a number by digits obtained by the subtraction of each digit from (r - 1) and adding 1 to the lowest digit.

Dopustimyi koeffitsient obrashchenii (Admissible conversion coefficient). The number of recordings or readings at a given spot on the screen of a storage tube above which inadmissible distortion of charges in neighbouring spots begins, and regeneration is required (see Vosstanovlenie). The admissible coefficient of conversion must be accompanied by an indication of the capacity of the store and the frequency of conversions for which this coefficient is fixed.

Emkost' khraneniya (Store capacity). The number of reliably distinguishable stable states of the physical medium used to store information.

Znak (Sign). Symbol representing the algebraic sign plus or minus.

Informatsiya (Information). Data expressed in language or as symbols and physical phenomena to which a determinate value is given. The transfer and storing of information

is brought about by means of material physical phenomena, electrical charges, ultrasonic pulses, punched holes, etc.

Klyuch (Key). A simple circuit or block designed for switching as a result of the logical operations AND, OR, NO-YES, etc. An output signal is given by the key when, and only when, a determinate combination of signals is applied to the input. The terms "ventil'" (valve) and "klapan" (valve, vent) are not recommended.

Kod (Code). A system of symbols used to present information in a machine. It may be a system of electrical pulses, charges on the screens of cathode ray tubes, states of electrical circuits, magnetization of a ferro-magnetic medium, perforations on paper tapes or cards, etc. Codes are of three kinds, classified according to the method of feed: parallel, when the digits are given simultaneously; serial; and mixed, containing parallel-serial feeds. For numbers we use, besides direct codes: a) inverted code, obtained by replacing each digit by its complement to $(r - 1)$, where r is the radix; b) complementary code, obtained by adding 1 to the lowest digit of the inverted code of the number.

Kodirovanie (Coding). The operation of presenting information in accordance with an accepted system of symbols.

Kod znaka (Sign code). The code used to represent the algebraic sign of a number.

Kod chisla ili komandy (Number or instruction code). A number or instruction presented in coded form, and consisting of a determinate number of digits. A unit of information in a machine. Synonym: "slovo" (word).

Komanda (Instruction). Indication of the form of an operation to be carried out by the machine on coded information, the address of which is given in the address part of the instruction. This indication is presented in the form of a digital code. A set of instructions set up on the basis of a chosen mathematical method forms the programme for the automatic solution of a problem; it usually contains one or more addresses for the information on which the operations are to be carried out. Synonyms: "instruktsiya", "prikaz" (order).

Kontrol' (Check). Checking and exposure of errors and dislocations in the working of a machine or programme.

Logicheskii kontrol' (Logical check). Check of working by logical means, including the mathematical method of interconversion ("two-handed") calculation of one and the same problem by different methods, comparing results with previously calculated exact supporting values, etc.

Profilakticheskii kontrol' (Preventive or marginal check). Means for early detection and replacement or adjustment of elements and assemblies which are faulty or in a condition not far from faulty. It combines technical and simple logical methods of checking.

Kontrol'naya tsifra (Check digit). A digit (sometimes several digits) introduced into the code of a number to detect faults in the calculation process.

Logicheskie operatsii (Logical operations). Operations having reference to operations in the field of mathematical logic. In automatic digital machines such operations are: comparison, selection, and sorting of data according to attributes; changing the properties of one number in accordance with the properties of another; determination of the next instruction, etc.

Masshtabnyi koeffitsient (Scale coefficient). The coefficient which secures modification of quantities taking part in calculations and quantities obtained within the admissible limits of representation of numbers in the machine.

Nakopitel' (Accumulator). A part of several types of arithmetical unit, designed for the storage of numbers. When other numbers are fed into the accumulator, an algebraic sum takes place in it. It contains a register, in which shift can take place, and is capable of forming complements. Synonym: "nakaplivayushchii summator" (accumulating adder).

Normalizatsiya (Normalization). An operation realized by a shift of the digits of a number to the left or right, as a result of which a non-zero number appears in the first digit place of the digital part of the number (mantissa) to the right of the decimal point.

Okruglenie (Rounding off). Discarding the least significant digits of a number, while observing the rules for increasing the exactness of the remaining part of the number.

Operatsii (Operations). Actions in a calculating machine having the aim of realizing arithmetical, logical, and other steps of the calculation. An operation appears in the instructions in code form.

Osnovanie schisleniya (Radix). The number $r \geqslant 2$, by means of which rational numbers are presented in the form of the polynomial $\sum a_n r^n$, where the coefficients a_n are whole numbers determined by the inequality $0 \leqslant a_n \leqslant r-1$; n are whole numbers denoting the number of the place (digit place) of the coefficient a, and indicating the power of the radix r. Systems of calculation are named according to the radix, (binary, ternary, ..., octal,..., decimal, ..., duodecimal, etc.). The usual form of writing numbers is by position: $\ldots a_n a_{n-1} \ldots a_1 a_0$, $a_{-1}\, a_{-2} \ldots$ The decimal point divides the whole part (positive powers of the radix) from the fractional part (negative powers of the radix).

Ostanov (Stop). Cessation of working specified by the instruction "stop" in the programme, and also as a result of the appearance of faults, or of the codes exceeding the limits of numbers representable in the machine ("avariinye ostanov", emergency stop).

Oshibka okrugleniya (Rounding-off error). An error arising in consequence of rounding-off.

Parallel'naya peredacha (Parallel feed). System of feeding information in which the digits of the code of a number or instruction are fed simultaneously, each by its own channel.

Plavayushchaya zapyataya (Floating decimal point). A means of presenting numbers, or of dividing the whole from the fractional part, in which the position of the decimal point in the number is not fixed, and can be changed automatically in the course of calculations. With this method, numbers are represented in the form of a power or order exponent and a mantissa or digital part of the number. For instance, the number 257 can be presented in the decimal system as 3 (power exponent) and 0.257 (mantissa), and in the binary system as 1001 (power exponent) and 0.100000001 (mantissa). The transposition of the decimal point by one digit place to the left is accompanied by an increase of the power exponent by one, and transposition to the right by a decrease. In many

machines with a floating decimal point it is not necessary to provide for change of scale of numbers in the process of a calculation. Unlike the system with a fixed decimal point, in this system any number within the limits of the number of digits that can be presented in the machine can be presented as the full number of significant digits.

Perenos (Carry). A process in counters and arithmetical units in which, as a result of adding, the sum of two digits in a digit place is greater than or equal to the radix, and a carry digit is added to the left-hand digit.

Posledovatel'nyi, ili kaskadnyi perenos (Successive, or cascade, carry). The process of feeding a carry digit successively from one digit place to the next to the left.

Skvoznoi perenos (Through carry). The process of feeding a carry digit, leaving out digit places in which the addition of the carry digit can give a sum greater than or equal to the radix.

Perepolnenie (Overflow). The state of counter circuits when the result of an arithmetical operation exceeds in number of digit places the capacity of the register in which the result is obtained.

Podprogramma (Subroutine). A part of a programme necessary for the fulfilment of a complex of determinate and frequently occurring mathematical and logical operations.

Pozitsionnyi sposob predstavleniya chisel (Position method of presenting numbers). One of the systems of presenting numbers by a determinate sequence of distribution of the digits composing these numbers. The digits indicated are coefficients of the powers of the radix. (See Osnovanie schisleniya).

Poleznoe vremya mashiny (Useful lifetime of a machine). The total time that a machine is in working condition, not including time of preventive adjustment and elimination of random faults.

Polusummator (Half adder). A circuit with two input and two output channels for binary signals (0 and 1) in which input signals, A and B, and output signals, S (sum) and C (carry), are interconnected as shown in the diagram. Two half-adders can form an adder.

Programma (Programme). A sequence of instructions so

drawn up that they secure the automatic carrying out of the arithmetical and logical operations necessary for the solution of a problem.

Input	A	0	0	1	1
	B	0	1	0	1
Output	S	0	1	1	0
	C	0	0	0	1

Ispytatel'naya programma (Test programme). A special programme designed for the detection of faults in the circuits of the machine or in other programmes. Synonym: "diagnosticheskaya programma" (diagnostic programme).

Programmirovanie (Programming). Design of programmes consisting of the selection of a numerical method of solution of a problem and its breakdown into a sequence of instructions. This sequence is then coded and fed into the machine.

Avtomaticheskoe programmirovanie (Automatic programming). Designing a programme by the use of a machine.

Proizvoditel'nost' mashiny (Productivity of a machine). The speed of calculation, including the time taken for input and output of information.

Pul't upravleniya kontrolya (Control desk). The part of a computer where the operator brings about the start, supervision, and stopping of the working of the machine.

Razryad (Digit place). The number of the place occupied by a digit. In the position method of forming numbers it corresponds to the power exponent of the radix (see Dvoichnyi razryad).

Registr (Register). A circuit or assembly designed to hold codes. Registers are used for buffer storage of information with a short delay time, and also to carry out operations in the arithmetic unit.

Registr so sdvigom (Shift register). A register in which information can be displaced one or more digit places to the right or left. It can be used to convert the feeding of codes from parallel to serial and vice versa.

Staticheskii registr (Static register). Register without shift.

Sdvig (Shift). Displacement of codes one or more digit places to the left or right.

Arifmeticheskii sdvig (Arithmetical shift). Displacement of codes equivalent to multiplication or division by a power of the radix.

Skorost' vychislenii (Speed of calculation). The number of arithmetical operations (such as addition and multiplication) in a unit of time, including the necessary references to the operative store.

Sravnenie (Comparison). A logical operation intended to find out whether a given code does or does not correspond in characteristics with that being compared with it. The result of this operation can be used for the automatic determination of the further course of the solution of the problem. Comparison of codes of numbers is usually carried out by the absolute values of the codes and by the sign. In some types of machine a special electrical circuit is allocated for this operation.

Standartnyi blok (Standard block, building block). The basic component of a computer, usually in the form of a dismountable, interchangeable unit.

Standartnaya programma (Standard programme). A programme for a whole series of frequently-occurring functions and problems.

Stiranie (Erasing). Destroying or clearing information in storage units before replacing it by new information.

Summator (Adder). A component of an arithmetic unit by means of which the algebraic summation of two or more numbers takes place.

Schetchik (Counter). A circuit or group of circuits in which the state of elements can be changed from one state to other successive states by the operation of every discrete signal fed in, in such a way that this process of changing the state is equivalent to counting.

Schetchik komand (Instruction counter). A counter in the control unit specially assigned for the counting of instructions.

Schityvanie (Reading). Output of information from a store.

Tochnost' predstavleniya chisel (Accuracy of representation of numbers). The limited number of digit places in numbers on which calculation can be carried out.

Trigger (Flip-flop). Electronic relay with two stable states, either of which it can assume under the influence of electrical control signals. Used in counting and switching circuits.

Uslovnyi perekhod (Conditional transfer). Instruction for automatic transfer to one of two other instructions in a programme, with indication of the address of the latter, which depends on certain properties of the numbers.

Ustroistvo avtomaticheskogo upravleniya (Control unit). A part of a computer allocated to the control of the order of working of all the other parts of the machine in accordance with the programme. The employment of the shorter terms "automatic control" or "control" is recommended.

Ustroistvo khraneniya (Storage unit). The part of a computer in which information is received (written) for storage, and whence it can be given out (read) later on. The shorter term "store" is recommended.

Operativnoe ustroistvo khraneniya (Operational store) A unit immediately connected with the arithmetic unit for automatic arithmetical and logical operations. Synonym: "vnutrennee ustroistvo khraneniya" (inner store).

Bufernoe ustroistvo khraneniya (Buffer store). An intermediate unit connecting the rapid-access operational store with an external store of slower access. It receives information at high speed from the operational store and subsequently delivers it at the working speed of the outer store, and vice versa.

Vneshnee ustroistvo khraneniya (Outer or backing store). A unit not immediately connected with the arithmetic unit. The input and output circuits of the machine usually appertain to the outer store.

Dinamicheskoe ustroistvo khraneniya (Dynamic storage unit). A unit in which information is kept in the form

of pulses in a physical medium.

Dopolnitel'noe ustroistvo khraneniya (Supplementary store). A unit designed for increasing the capacity of the operational store.

Staticheskoe ustroistvo khraneniya (Static store). A unit in which the information stored is not in movement through a physical medium.

Ustroistvo khraneniya na liniyakh zaderzhki (Delay line storage unit). A unit in which electromagnetic, ultrasonic, or other delay lines are used to store information.

Ustroistvo khraneniya na magnitnom barabane (Magnetic drum storage unit). A unit in which information is recorded on the magnetized surface of a cylindrical drum revolving about the longitudinal axis.

Ustroistvo khraneniya na magnitnykh serdechnikakh (Magnetic core storage unit). A unit in which information is represented in the form of magnetic states of simple magnetic cores.

Ustroistvo khraneniya na potentsialoskopakh (Cathode-ray tube storage unit). A unit in which information is stored in the form of discrete electrostatic charges formed by the beam current on the target of a tube. Usually used as an operational (inner) store.

Fiksirovannaya zapyataya (Fixed decimal point). A method of presenting numbers, or dividing the whole from the fractional part, in which the position of the decimal point in the number is fixed. In this case, change of scale of the numbers used and obtained in the course of calculation has to be provided for. (See Osnovanie schisleniya and Plavayushchaya zapyataya).

Formirovatel' (Shaper). An electrical circuit by means of which signals received are given the specified form.

Tsiklmashin (Machine cycle). The time between the end of one operation and the beginning of another, in the course of which one instruction is carried out, including the selection of instruction and number codes and carrying out of the operation.

Tsifra (Digit). One of a determinate series of symbols of quantity used to form numbers. With the position method of presentation (see Pozitsionnyi sposob) the digits are coefficients of the powers of the radix.

Yacheika khraneniya (Storage cell). Place in a storage unit in which the code of a number of instruction is to be found, usually indicated in the form of an address (number).

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